Low Variability Layout Solutions For Maximizing Benefits of FDSOI Technology

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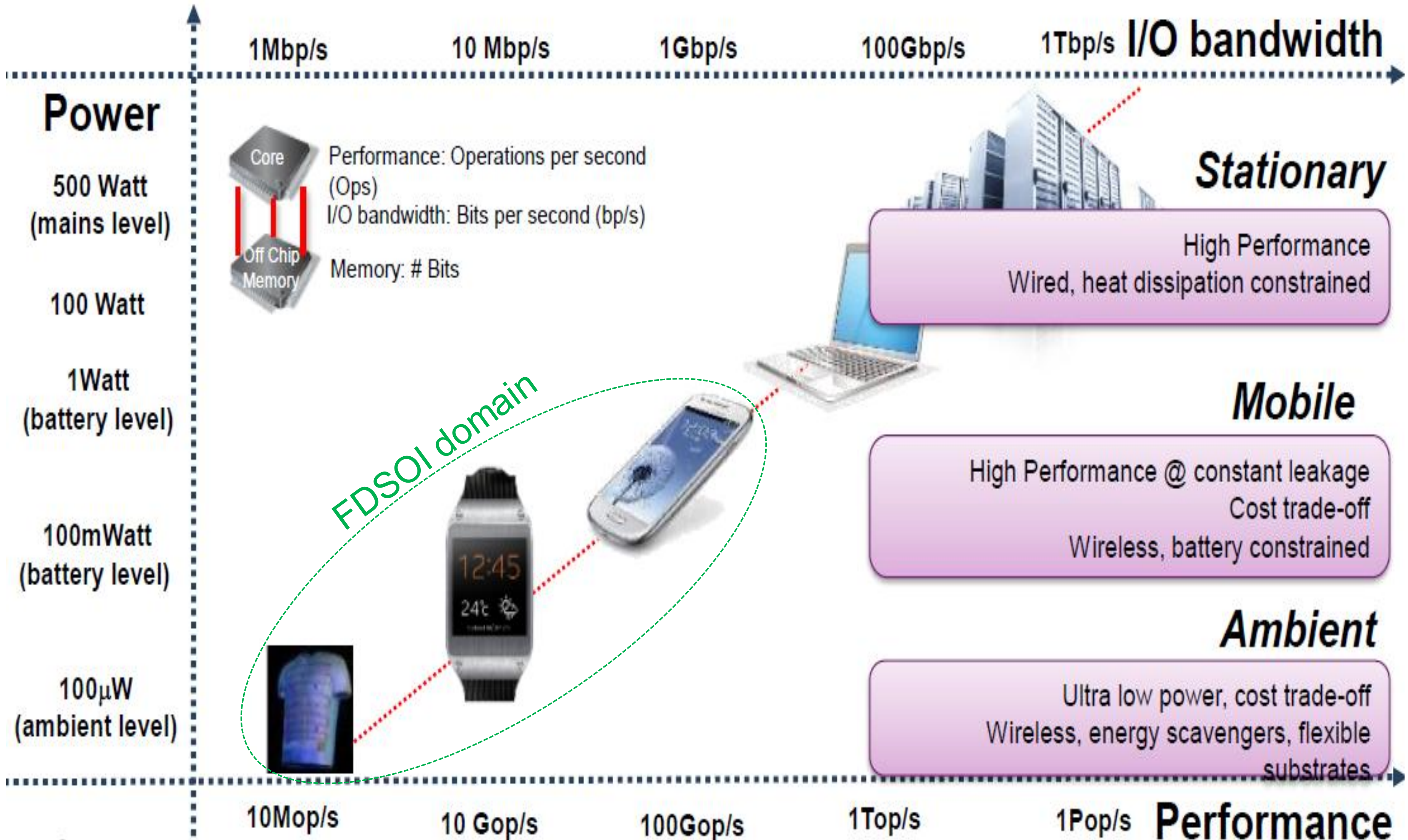
IoT Device Landscape



Source: G. Jurczak, IMEC, CSTIC -2015

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Mobile Platforms and Big Data Analytics: Reason for Scaling

High Volume
Peta-byte to Exa-byte

Rich
Audio, video, transactions,...

Dispersed
Local, cloud, real time

Varying Fidelity
Useful data, and lots of junk!

Process locally & globally
Mining and inference

Source: S. Borkar, Intel, VLSI -2015

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IoT Roadmap Summary

- IoT: Trillion connected devices must be supported
- Wireless Ultra Low Power Sensors and Energy Harvesters do not require advanced technology nodes: 55, 40, 28 and 22nm will suffice
  - Inexpensive 22 nm FDSOI w/mixed signal/RF looks very attractive
- However, Mobile Platforms and Servers for Big Data Handling will push scaling to 5nm and below
  - FinFETs and Nanowires scalable to 3nm but then devices not based on charge transport must be implemented
- Extreme layout regularity required for FEOL, MOL and even BEOL to reduce the number of layout patterns
  - Complex local interconnect required
  - Litho/process integration choices impose extremely regular 1D patterns
  - Design Technology Co-Optimization becomes critical to control printability, manufacturability and variability control

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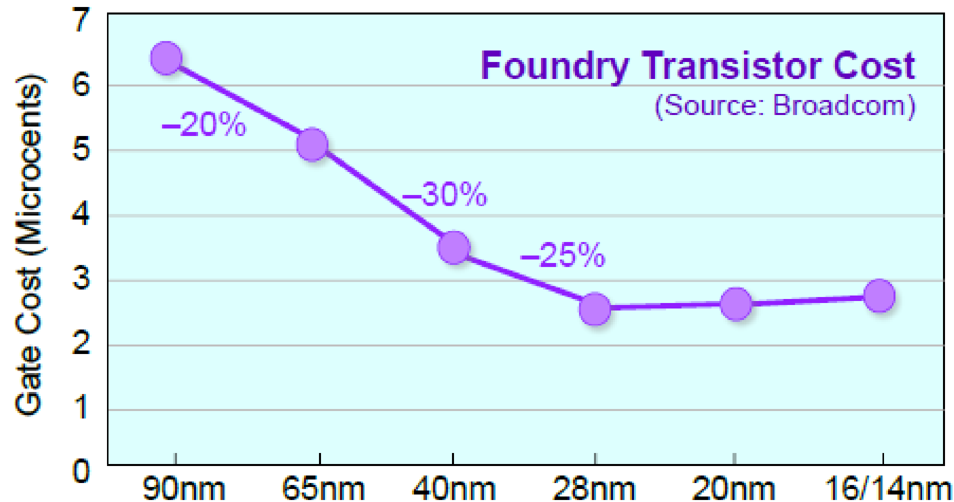
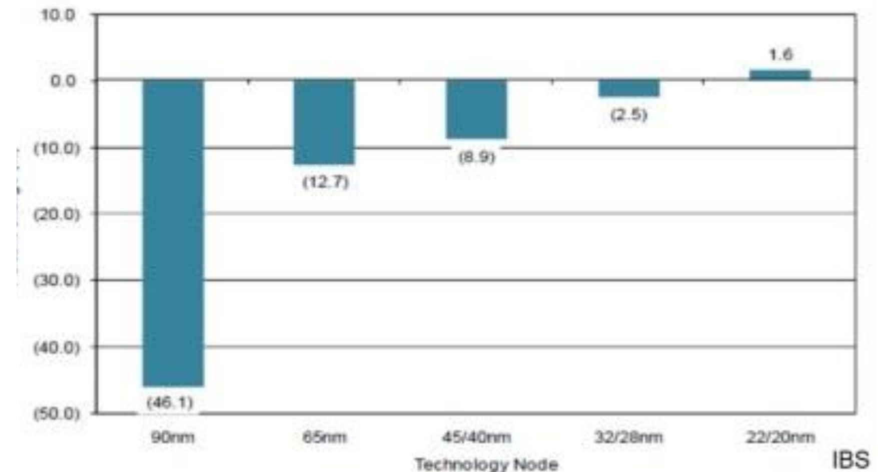
Economy of "scaling"

- **Complex integration scheme and lack of new litho solution drive the cost up**
  - Linear/Area scaling less than historical (0.7x)
  - Performance Gain below expectations…
  - Current processing cost very high and depreciation does not guarantee fast X-over and further cost reduction





Diminishing benefit of cost reduction from dimensional scaling – at 20nm node the Cost/Gate goes up…

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New Technology, New Opportunities, Old Habits?

- 22nm FDSOI has the opportunity to be the superior technology to address ultra low power, low cost markets
- From a technology optimization perspective, the Internet of Things applications should be built on FDSOI
- One of the biggest risks to this opportunity is “old habits”
  - Small parts tend to be pad limited: Power-Performance-Area (PPA) -> Power-Performance-Yield (PPY), where systematic yield, process margin, and parametric yield trump cell area
  - Design style diversity -> channeling layout into controlled sweet spot of layout patterns
  - “Blind simulation” power/timing optimization -> Si centric power/timing optimization

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22nm FDSOI: Opportunities and Challenges

- **FDSOI has the potential for providing a low variability technology, however achieving that potential requires tight control of sources of variation that contribute to global variation**
  - Combination of best in class global variation and lower local variation allows FDSOI technologies to have best in class variation, enabling ultra-low power and compact designs
  - However, best in class process control in manufacturing is essential to achieve FDSOI's potential, the local variation benefits from the intrinsic transistor design may be lost by sub-optimal process control contributing to global variation

- **FDSOI technology is sensitive to new sources of variation, innovations in characterization and control are required to minimize the impact of these new sources of variation**
  - Example: sensitivity to silicon thickness
  - New methods for fast and accurate characterization of Tsi and its impact have been developed

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FDSOI Promises Variability Reduction, Crucial for ULP

- **Benchmarking data so far look promising (transistor variability already lower than 28HKMG bulk)**
- **However, all 28nm and below technologies have variability issues due to small process windows and local layout effects**

	28 bulk	14FF	FDSOI	Solutions for FDSOI
Process control	Random dopant fluctuations	Fin height & width variations	Tsi variations	Institute electrical test structures for characterization of incoming substrate & in process thickness control
Layout effects	Too many layout patterns	Too many layout patterns	Too many layout patterns	Reduce layout pattern set to eliminate risky patterns
Si vs SPICE	Too many Tx neighborhoods	Tx termination styles	Effects of active breaks	Eliminate high variability patterns
Leakage tails	Too many high risk patterns	Too many high risk patterns	Too many high risk patterns	Eliminate high risk patterns

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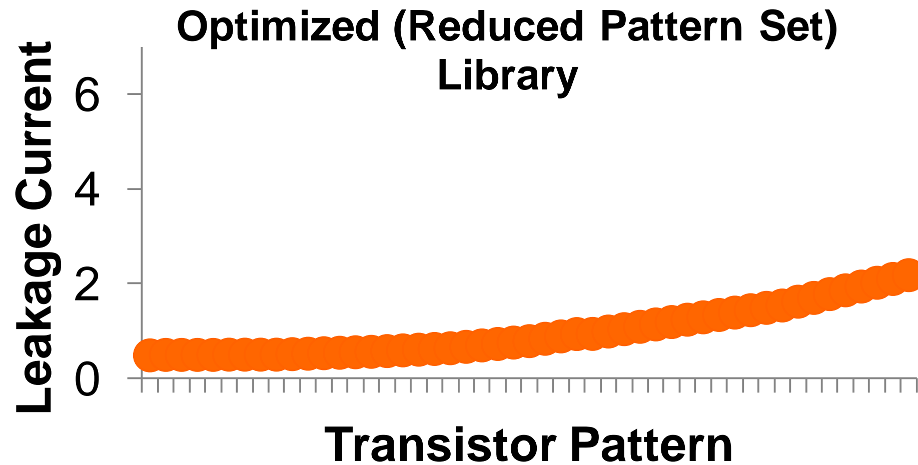
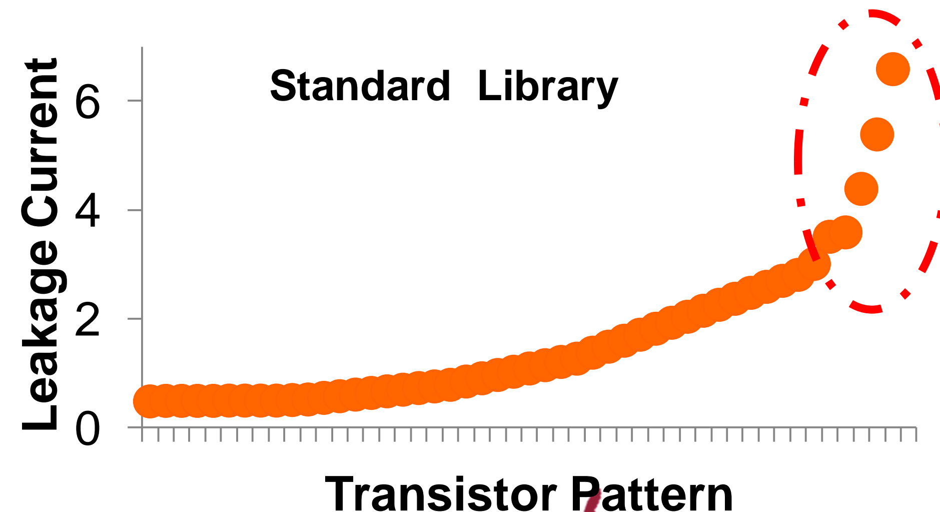
Leakage Optimization by Layout Pattern Restriction

- Chip leakage is dominated by a small number of tail transistors of the exponential curves
  - Leakage follows exponential curve
- Comprehensive statistical characterization can identify all unique layout patterns that cause the leakage tails in the standard cell libraries and ensure that these transistor layout patterns are avoided





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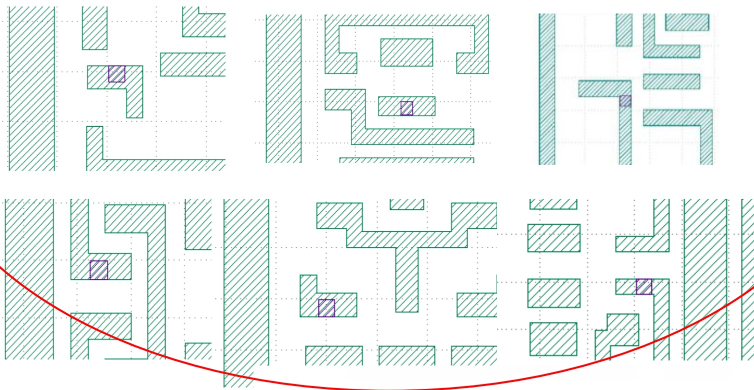
Pushing High Risk Layout Patterns: Not Worth It

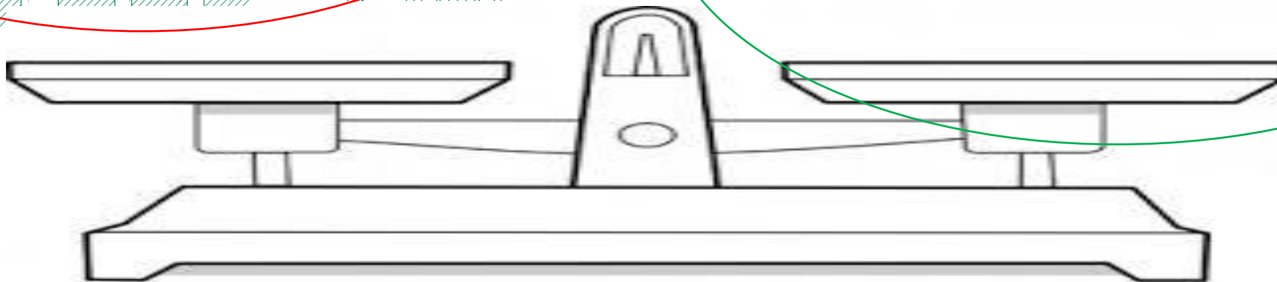
- **Old tricks to push rules and shrink cell area by 1% are not worth it in FDSOI where process window, TTM, and systematic yield dominate**

High Yield Risk Layout Patterns



vs.

- Process window improvement
- Time to market improvement
- Systematic yield improvement



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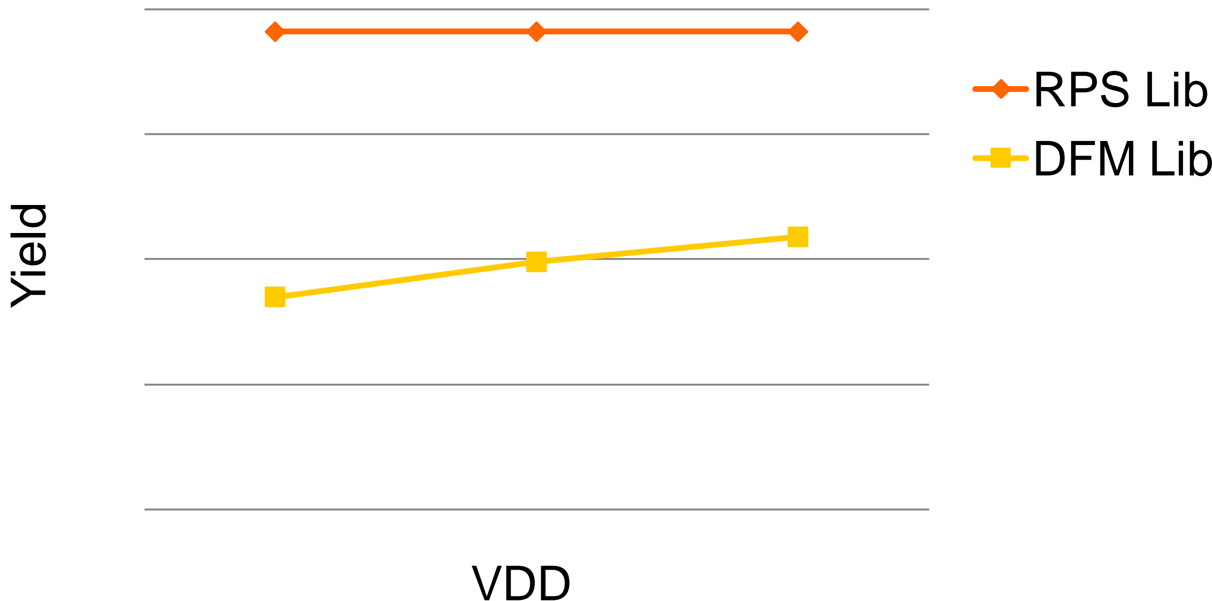
Costs Directly Proportional to Process Window

- Dies at edge of wafers tend to be exposed to wider process variations and account for 1/3 of all Dies on Wafer
- For dies at wafer edge, reduced pattern set libraries show better yield and more stable yield across VDD

Yield vs. VDD:
Only Including Wafer Edge Die



Dies considered "Wafer Edge" shown in red

Y										
7				1	1	1	1			
6		1	1					1	1	
5	1				1	1				1
4	1		1	1	1	1	1	1		1
3	1		1	1	1	1	1	1		1
2	1				1	1				1
1		1	1					1	1	
0				1	1	1	1			
	0	1	2	3	4	5	6	7	8	9
	X									

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Layout Regularity Key to Cost Reduction and TTM

Limiting Number of Layout Patterns Allowed Intel to Significantly Reduce TTM for 32nm and Introduce FinFETs at 22nm

Contacted Gate Pitch (nm)

250
200
150
100
50
0

2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015

Intel
Foundries

65nm
Poly: 1D

45nm
Poly: Gridded layout,
single pitch,
comp lithography

32nm
Immersion
lithography

22nm
SADP for active
fixed-width fin

14nm
SADP for active
fixed-width fin

40nm
Immersion
lithography

28nm
Poly: Gridded layout,
single pitch,
comp lithography

20nm

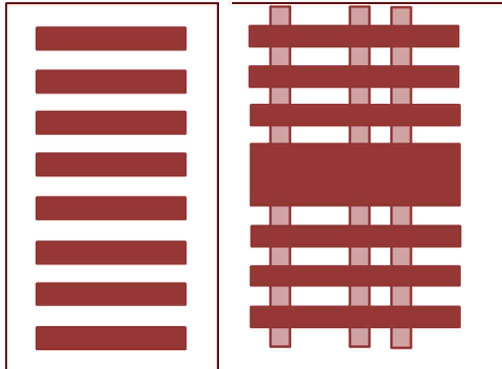
14nm
SADP for active
fixed-width fin

Source: D. Kanter, The Linley Group Report, August 31, 2015

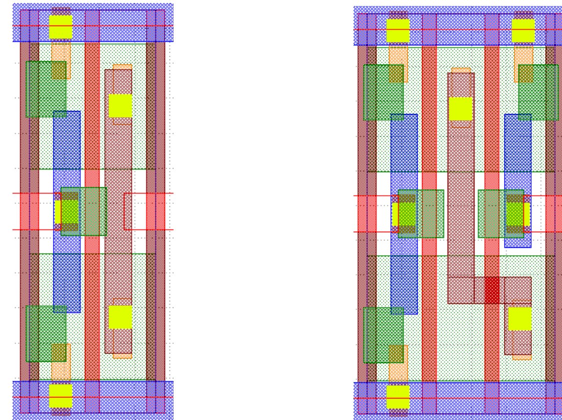
DTCO Flow – Ground Rules To Layout Constructs

Process Ground Rules

Layout Constructs



•Basic process capabilities are quantified resulting in allowed pitches and ground rules



• Layout constructs that exercise the required layout space
• Reduced Pattern Set cells for evaluation

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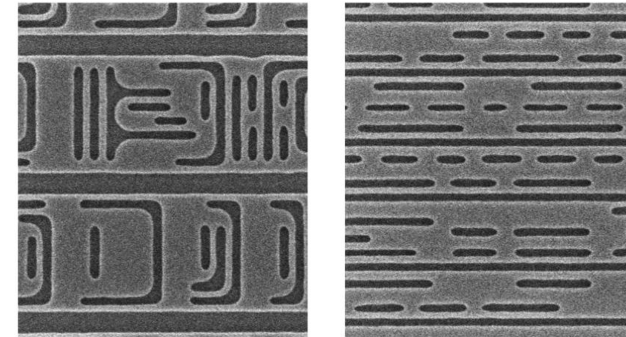
Reduced Layout Pattern Set Development and Evaluation

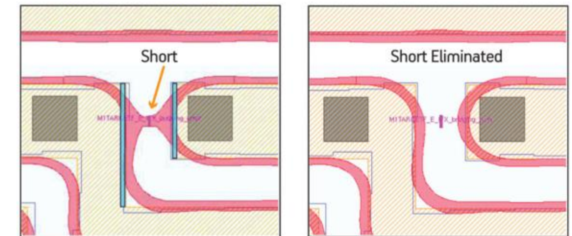
Litho

- Find process window
- Identify weak points in simulation



Si

- Test structures to isolate critical patterns
- Test structures to examine tradeoffs between issues



Parasitics

- Check parasitic implications
- Identify parasitic hotspots

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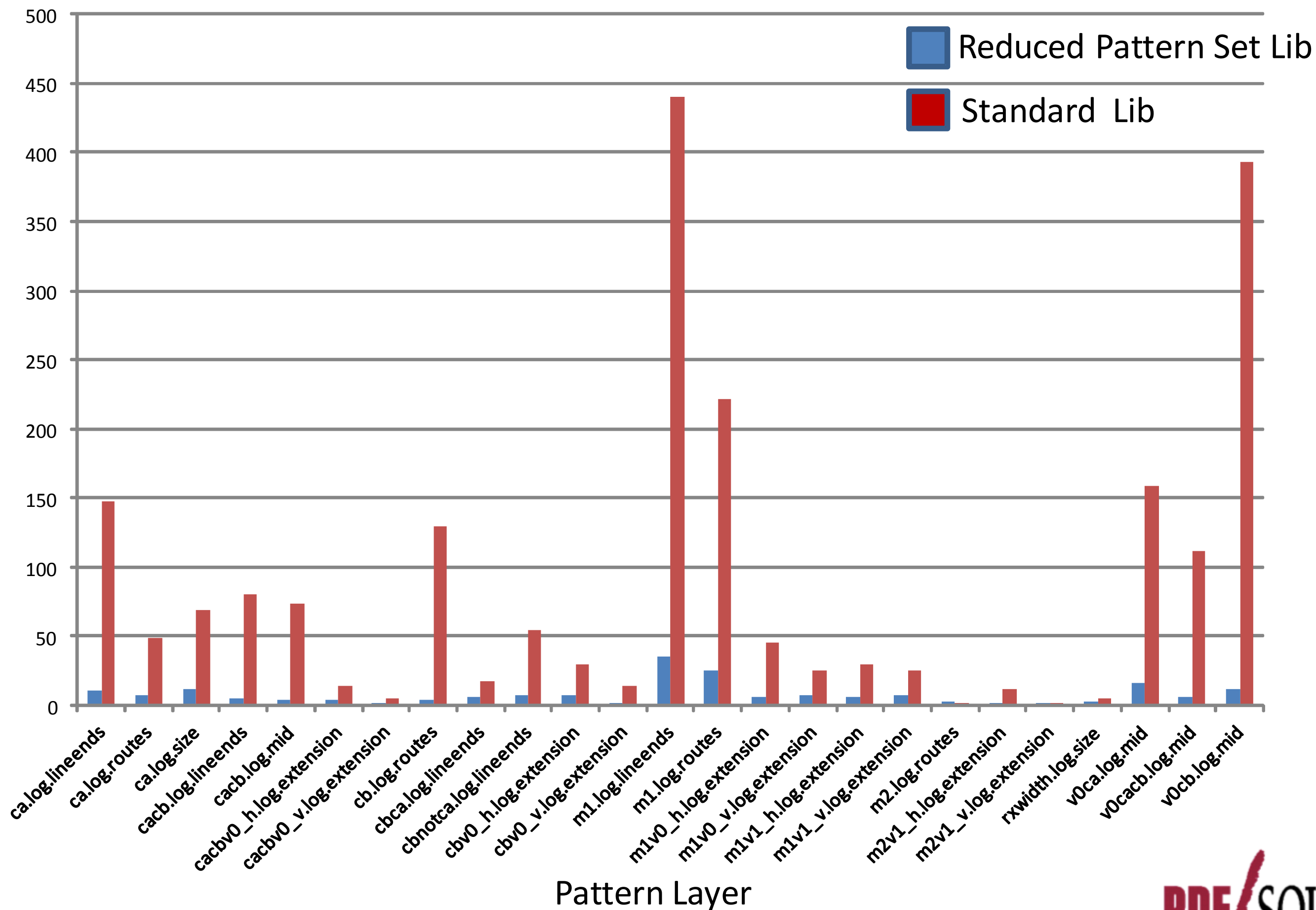
Tighter Corners Come From Tighter Layout!



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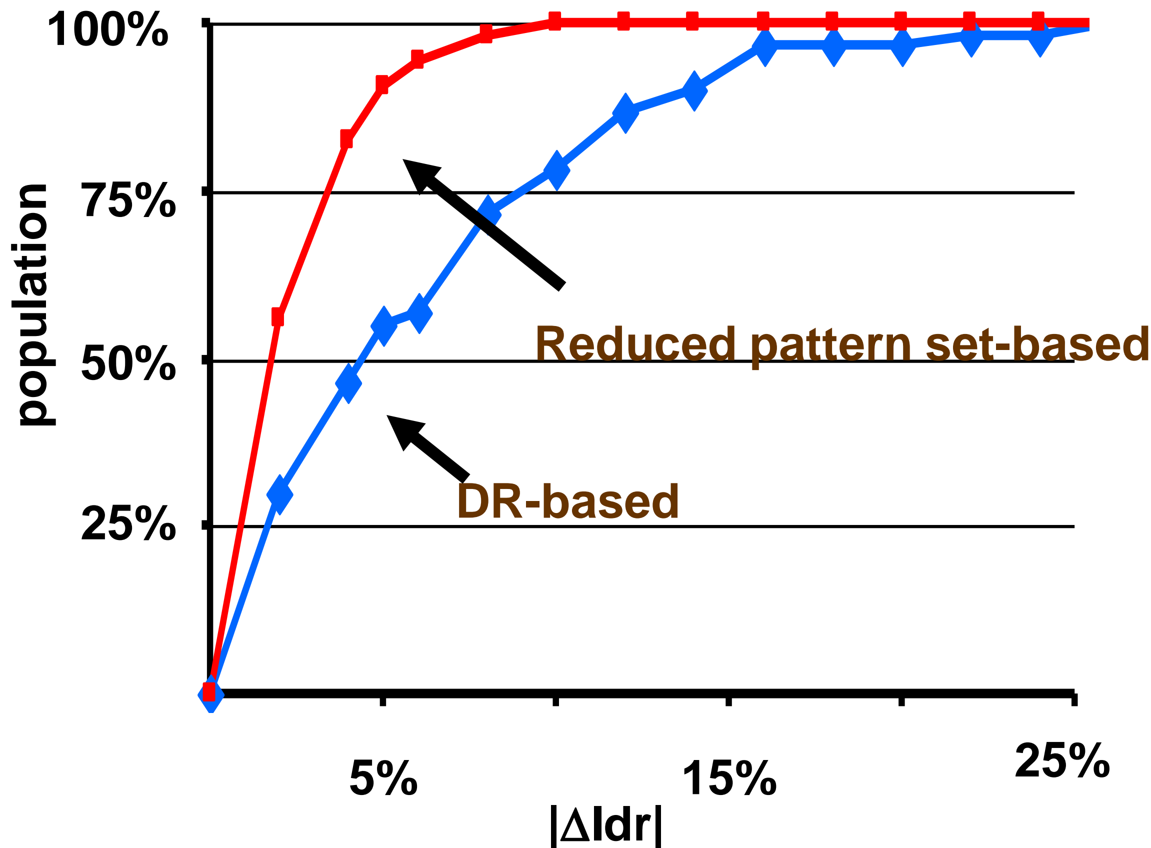
Fabless Benefit From Reduced Pattern Set Low Variability



- Significantly tighter transistor performance distribution achieved by limiting transistor neighborhoods
- SPICE models show up to 30% errors vs. silicon across DR legal layout space
  - Reduced Pattern Set approach limits device neighborhoods and enable calibrating models for finite set of device patterns

28nm example data shown

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Conclusions

- 22nm FDSOI has a great potential for providing ultra low power, low cost and low variability solution for IoT
- Thorough understanding and characterization of local and global variation sources is key to achieve efficient technology ramp and time to market for leading products
- Drastic reduction of the layout pattern set is absolutely necessary for comprehensive and timely characterization in Silicon and development of robust PDK for the fabless community
- Power-Performance-Yield should become the new metric for 22nm FDSOI success in the marketplace

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