Enabling Next Generation Innovation with 22FDX™

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Growth in Mobile Computing

Drivers of growth
- Emerging markets
- Social
- eCommerce
- Machine-to-machine interaction
- 5G
- Content consumption

Requirements of semiconductors
- Cost
- Performance equivalent to today’s high-end smartphones
- Power consumption

Cost and Energy Efficiency will be Key Drivers of Innovation
Development of Pervasive Computing

All devices are *connected* and *share* their sensor state with the Internet to *optimize* computing.

Drivers of growth
- Increased network bandwidth
- Big data/analytics services
- Simple user interface
- Security and privacy

Requirements of semiconductors
- Ultra-low power consumption: order of magnitude lower
- Cost: ASP equivalent to $1

Cost and Energy Efficiency will be Key Drivers of Innovation
Emergence of Intelligent Computing

**Elements**
- Natural interface
- Real-time decision-making
- Ambient
- Sensory
- Aware
- Always on

**Drivers of growth**
- Drones
- Automotive
- Robotics

**Requirements of semiconductors**
- Ultra-high performance: e.g. 60 fps image processing
- Very low power
- Cost

Cost and Energy Efficiency will be Key Drivers of Innovation

Connecting Everything Everywhere

- Ambient Sensors
- IoT
- Smart Everything Everywhere
- Autonomous Cars
- Drones / Robots
- Smartphones
- Wearables
- Wireless Network
- Cloud
COST: The economic foundation on which the semiconductor industry has functioned for 4 decades – is at risk…

Wafer cost increase driven by scaling and compounded by - FINFET and double patterning requirements

The era in which shrinking features automatically ensured cheaper transistors is over!

Historical First: Cost per Transistor is Rising
Energy Efficiency: 0.4V is the Minimum Energy Point for almost any Technology – 22FDX™ gets you there..

Most optimum energy operating point is around 0.4V
- As Vdd decreases dynamic power goes down drastically while frequency also goes down
- Leakage power also goes down as Vdd drops
- Energy goes up below ~0.4V Vdd since delay increases result in crow-bar current increase, overshadowing dynamic power reduction
SRAM remains functional down to $V_{DD}=0.4V$

FDSOI 0.08um2 SRAM (80nm CPP)

- SRAM Stability and $V_t$ Variability Improvement with Back Bias
- Clear SNM modulation from back bias
- Both Stability and $V_t$ variation improved with RBB

Qing Liu, et al., VLSI
FinFET & FD-SOI Solve Different Market Needs

Bulk CMOS
- Lowest Cost
- Fully Depleted Channel for Low Leakage

Ultra-thin Buried Oxide Insulator

FinFET
- High Performance
- SOURCE
- GATE
- INSULATOR
- DRAIN
Introducing 22FDX™ Platform

• Industry’s first 22nm fully-depleted silicon-on-insulator (FD-SOI) technology
• Delivers FinFET-like performance and energy-efficiency at 28nm cost
• Ultra-lower power consumption with 0.4 volt operation
• Software-controlled transistor body-biasing for flexible trade-off between performance and power
• Integrated RF for reduced system cost and back-gate feature to reduce RF power up to ~50%
• Post-Silicon Tuning/Trimming
• Enables applications across mobile, IoT and RF markets

- 70% lower power than 28HKMG
- 20% smaller die than 28nm bulk planar
- Lower die cost than FinFETs
22FDX™ Offers the widest range of Performance/Leakage Optimization points

**Relative Performance**
- 1.0
- 0.8
- 0.6
- 0.4
- 0.2
- 1.2

**Relative Leakage**
- 0.0
- 1
- 10
- 100
- 1000
- 10000
- 100000
- 1000000

**SLVT/LVT**
- Lowest $V_T$
- Optimized for FBB
- Highest performance

**RVT/HVT**
- Mid-range $V_T$
- Optimized for RBB
- Balance of low leakage and high performance

**ULL**
- Optimized for leakage
- Coupled with RBB achieves $\approx1pA/\mu m$ leakage
22FDX™: Multiple Body-Bias and Vt Points on Same Die

Optimize Standby and Dynamic Power

Integrated RF

Wakes up comm block to transmit message

Wireless Comms

ON

“Watchdog” Processor

ON

ON

Wakes up Image Processor to zoom in and analyze

FD-SOI Delivers:

☑ Low static and dynamic power
☑ RF integration for reduced BOM cost
☑ RBB and FBB for power/perf tradeoffs
ARM Cortex A7 Implementation – Initial results

22FDX is the First Technology to demonstrate 0.4V operation capability at >500Mhz on an ARM A7 Processor

- FinFet like Performance (1.2Ghz)
- 50% faster performance and 18% lower power than 28HKMG
- 47% lower power than 28HKMG at Iso-Frequency

22FDX at 0.4v
- 92% Less Power at 520MHz (wrt 28HKMG at 800MHz)

Source: Verisilicon
22FDX™ Platform Extensions

- **22FDX Base Platform**
  - 4 Core Vts
  - 2 IO Vts @ 1.2/1.5/1.8v
  - Passives
  - SRAMs (HD, HC, LV, ULV, TP)
  - 8T/12T libraries
  - Software controlled Forward/Reverse body-bias

- **-ulp adds** logic libraries and memory compiler optimized for 0.4v logic operation

- **-ull adds** devices, libraries, and memory compilers to achieve 1pA/um leakage

- **-uhp adds** optimized BEOL stacks, 12T libraries optimized at OD, high-speed SERDES (16/28GHz), and MIM capacitor

- **-rfa adds** RF enablement, BEOL passives, and IP for BTLE, WiFi

Base platform PDK & IP

Application-optimized extensions
22FDX™ improved electrostatics enable higher operating $f_T$, higher self-gain at high gain efficiency bias

Each curve is constructed by simulating multiple $L_g$ for that technology. $V_g$ is swept and $F_T$ and self gain found for the $V_g$ where $g_m/I=15$ $V^{-1}$. The right most point on each curve is the minimum allowed $L_g$. Longer FETs have higher self gain and lower $F_T$. 
Cost Per Function and Energy Efficiency are the two most important metrics for next wave of Innovations.

22FDX™: Multiple Functions Integrated

22FDX™: Best Power, Performance

22FDX™ enables System level Integration without the need for multiple heterogeneous technologies.
Design Migration to 22FDX™ from Bulk node

Migration to 22FDX™ (Design Flow):

- **Design Planning** (FBB vs RBB)
  - Library Char + POCV/LVF variability
    - Lib char with BB (Added corners)

- **RTL Synthesis**
  - UPF Connectivity

- **Cell placement + Tapcell Placement + CTS pre-route**
  - Implant-aware

- **Routing Optimization**
  - Tapcell connections (BB mesh + HV rules)

- **In-Design Modules (DRC + PM + MetalFill + EMIR)**

- **Physical Verification + EMIR**
  - Sign-Off PEX/STA (+DPT extraction)
    - Optional: Add sign-off Corners for dynamic BB variables (PVTB)

- **Routing Optimization**
  - Leakage recovery with VT swapping + Lgate optimization
    - Optional: use FBB/RBB performance/power optimization

Nov 2015: Ansys, Atoptech, Cadence, Mentor, Synopsys announced EDA support for 22FDX™
Successful Early Collaboration (TechCon 2015): ARM Cortex-A17 Quad-core Implementation

- Successful Cortex-A17 quad-core implementation using:
  - 5 power domains (4 CPU cores + 1 nonCPU module)
  - 5 body-bias net pairs (n-well, p-well biasing)
    - 1 pair for standard cells
    - 2 pairs for L1 cache periphery, bitcell array
    - 2 pairs for L2 cache periphery, bitcell array
    - Body-bias nets might be shared depending on eventual IP features
- Used our reference flow capability
- Coming Soon:
  - Hierarchical low power flow (VDD and BB scaling control)
  - In-design added modules (DRC/PM/MetalFill)
  - Power and signal EMIR modules
  - Integrate BB IP to generate the bias voltages
## 22FDX™ Foundation IP – Under Development

<table>
<thead>
<tr>
<th>IP Type</th>
<th>IP Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Foundation IP</strong></td>
<td></td>
</tr>
<tr>
<td>Standard Cells</td>
<td>High Density, High Performance</td>
</tr>
<tr>
<td>Memory Compilers</td>
<td>(a) High Density Single-Port SRAM</td>
</tr>
<tr>
<td></td>
<td>(b) High Speed Single-Port SRAM</td>
</tr>
<tr>
<td></td>
<td>(c) High Density Single-Port Register File</td>
</tr>
<tr>
<td></td>
<td>(d) High Speed Single-Port Register File</td>
</tr>
<tr>
<td></td>
<td>(e) High Speed Two-Port Register File</td>
</tr>
<tr>
<td></td>
<td>(f) High Density Via ROM</td>
</tr>
<tr>
<td>GPIO</td>
<td>Voltages TBD and interfaces (SPI, I2C, MMC)</td>
</tr>
<tr>
<td>eFuse</td>
<td>4K macro</td>
</tr>
<tr>
<td>PLL</td>
<td>2-3 PLLs; Frequency, Jitter, Area, Power TBD</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>Support for multiple remote monitors</td>
</tr>
<tr>
<td>OTP</td>
<td>One-Time Programmable</td>
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</tbody>
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# 22FDX™ Complex IP – Under Development

<table>
<thead>
<tr>
<th>IP Type</th>
<th>IP Description</th>
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</thead>
<tbody>
<tr>
<td>Complex IP</td>
<td></td>
</tr>
<tr>
<td>1-12.5G Multi-protocol</td>
<td>PCIe 1.1 (x1); XAUI 3.125</td>
</tr>
<tr>
<td>SERDES</td>
<td>PCI2 2.0 (x1, x4); XAUI 6.125</td>
</tr>
<tr>
<td></td>
<td>PCIe3 (Root and endpoint 2.5/5.0/8.0Gb/s)</td>
</tr>
<tr>
<td></td>
<td>USB3.1 (5/10Gb/s)</td>
</tr>
<tr>
<td></td>
<td>SATA (Gen 1, 2, and 3)</td>
</tr>
<tr>
<td></td>
<td>Ethernet 1 – 10G BP KR</td>
</tr>
<tr>
<td>USB2 PHY</td>
<td>USB2.0 HOST and OTG</td>
</tr>
<tr>
<td>DDR3/DDR4</td>
<td>DDR3 up to 2400, DDR4 up to 3600</td>
</tr>
<tr>
<td>LPDDR3/LPDDR4</td>
<td>LPDDR3 2133, LPDDR4 4267</td>
</tr>
<tr>
<td>DPHY</td>
<td>MIPI DPHY (CSI2, DSI) [4lanes; 12 Bit]</td>
</tr>
<tr>
<td>MPHY or CPHY</td>
<td>MIPI MPHY (SSIC/UFS2) with Gear3 support</td>
</tr>
<tr>
<td>DP/HDMI/MHL 2.x – TX</td>
<td>Combo, HDMI2.x (6Gb/s), DisplayPort1.3 (8.1Gb/s)</td>
</tr>
<tr>
<td>DP/HDMI/MHL 2.x – RX</td>
<td>DisplayPort (5.4Gb/s), HDMI2.x (6Gb/s)</td>
</tr>
<tr>
<td>Frac PLL</td>
<td>1 GHz, Low Jitter PLL</td>
</tr>
<tr>
<td>Video DAC</td>
<td></td>
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<tr>
<td>24b Audio DAC</td>
<td>2-Channel</td>
</tr>
<tr>
<td>16b SAR Audio ADC</td>
<td>2 Channel</td>
</tr>
<tr>
<td>Body Bias Generator</td>
<td>Modular Design</td>
</tr>
<tr>
<td>RF IP</td>
<td>WiFi (802.11AC), 802.15.4, Blue Tooth LE</td>
</tr>
</tbody>
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FDSOI – The Road Ahead
22FDX™ Differentiated features will be extended to 10nm Generation

<table>
<thead>
<tr>
<th>FDSOI Scaling</th>
<th>FinFET Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strong industry support today – Ecosystem being established on an accelerated pace</td>
<td>Ecosystem established</td>
</tr>
<tr>
<td>Scaling roadmap</td>
<td>Scaling roadmap</td>
</tr>
<tr>
<td>- Power/Perf demonstrated w/ 14FD</td>
<td>- Good electrostatic demonstrated</td>
</tr>
<tr>
<td>- Boosters defined down to 10FD</td>
<td>- Higher effective Device width</td>
</tr>
<tr>
<td>Lower Cost / Die</td>
<td>Higher Cost &amp; Higher complexity</td>
</tr>
<tr>
<td>- Fewer mask layers</td>
<td></td>
</tr>
<tr>
<td>- Faster learning cycles</td>
<td></td>
</tr>
<tr>
<td>Back-Gate bias (Software controlled)</td>
<td>Back Bias is not Effective</td>
</tr>
<tr>
<td>- Process / Variability compensation</td>
<td></td>
</tr>
<tr>
<td>- Flexible Dynamic vs. Static Power</td>
<td></td>
</tr>
<tr>
<td>Low-Leakage Devices &amp; Memory</td>
<td>Higher Leakage in a given foot-print (3D)</td>
</tr>
<tr>
<td>- Reverse body-bias enhances further</td>
<td></td>
</tr>
<tr>
<td>Lowest Vmin Device</td>
<td>Low Vdd, but inherently higher than FDSOI</td>
</tr>
<tr>
<td>- Lower intrinsic Capacitance</td>
<td>- 3D architecture required for electrostatics</td>
</tr>
<tr>
<td>- Lower intrinsic variability</td>
<td></td>
</tr>
<tr>
<td>- Superior Weff tuning for low power</td>
<td></td>
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<tr>
<td>- Forward body-bias</td>
<td></td>
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</tbody>
</table>
Scaling rules down to 7nm node

TCAD with Electrostatic considerations

![Graph showing scaling rules down to 7nm node](image)

Required T_{SOI} (nm)

TSOI (thick BOX=145nm)

TSOI (UTBOX case)

DIBL=100mV/V

NanoWire

T_{BOX}= 25nm

25nm

10nm

7.5nm

T_{BOX}= 145nm

5nm T_{si}

Courtesy of CEA-LETI, O. Faynot et. al. IEDM 2010
22FDX™: The Right Technology at the Right Time

Server

High Performance Computing & Switching

High-end Mobile Application Processor

Wired Networking, Consumer Applications Mid-Range Smart phone

IoT, Wearables, Sensors, Low-end Smartphone

22FDX™ Design Kits available NOW

Next node Target: 10nm FinFET Performance at 20-30% lower die-cost
22FDX™: Accelerates Innovation across a wide range of Applications

**Consumer (STB/DTV)**
Beats Energy Star goals and enables small form factors

**Mainstream Mobile**
Meets display, video, and wireless needs w/o FinFET cost

**Wearables**
Longer battery life and RF integration to reduce system cost

**Auto/Info-**
Lower $T_j$ at 125°C ambient and better Soft Error Rate (SER)

**IoT/Industrial (MPU, ISP, MCU)**
HD image/video, integrated RF/MRAM, battery operation

**WiFi/RF**
Achieves higher data rates at lower power
Enabling Next Generation Innovation with 22FDX™

22FDX™: The Right Technology at the Right Time

• FinFET-like performance at 28nm cost
• 0.4 Volt Operation offers the best energy efficiency
• Software-controlled transistor body-biasing enables Innovative Power Management schemes
• Integrated eNVM and RF enables lowest cost and smallest form-factor
• Post-Silicon Tuning/Trimming enables differentiation

Design Kits available now

Let us Lead the next wave of Innovations together!!
Thank you