RF SOI: Defining the RF-Digital Boundary for 5G

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Agenda

- 5G Overview
- Technical Challenges & Solutions
- RF SOI for 5G
What is 5G?

5G promises to deliver:

- Broadband user experience
- Improved cell edge performance
- High user density
- Improved spectral efficiency
- Reduced latency
- On-the-go connectivity
- High reliability and secure communications

5G Use Cases

5G will enable ubiquitous connectivity:

- Pervasive video
- Tactile internet
- E-Health
- IoT and sensor networks
- Broadcast services
- Automated vehicles
- Mission-critical communications

*mmWave is a key enabler in delivering the promises of 5G*

Source: “Bracing for 5G”, Pipeline, February 2015
5G Spectrum Candidates

Candidate frequency bands being considered for 5G:
- Below 6GHz
- Above 28GHz

Available spectrum above 28GHz gives mmwave an advantage:
- Greater density
- Higher data rate

…but is challenged by the reduced range due to atmospheric attenuation

Steerable phased arrays are needed for mmwave to concentrate the radiated energy

Source: “5G Ultra Wide band Enhanced Local Area Systems at Millimeter Wave,” Nokia, September 2013
5G Early Demonstration in Flight…

KT Telecom CEO committed to providing 5G commercial services for 2018 Olympics in PyeongChang, Korea

"It’s the next-generation network we need. Speed is only one part of the requirement, the biggest is capacity. We need to build a network that’ll be able to deliver real-time data with very low latency."

Chang-Gyu Hwang
CEO KT Telecom, MWC2015
Key Enabler for 5G Radios: mmWave Phased-Array Front End

LEO satellites for broadband communications

Future 5G handset & small cell

CMOS auto radar

mmWave backhaul

Short distance, highly focused antenna beam $\Rightarrow$ spatial multiplexing, less total TX power

TX power / array element $\Rightarrow$ TX power of power amplifier array $\Rightarrow$ lower power per element

All of these mmWave applications have one thing in common – phased array antenna system
mmWave Phased-Array Transceiver Architectures

Technology implications:
- TX power / power amplifier
- Receiver sensitivity & noise figure
- Phase noise of local oscillator
- System loss at mmWave:
  - Amplifier efficiency
  - Switch loss
  - On-chip routing loss (passives & T-lines)
  - Off-chip routing loss (package, board)
- mmWave design requires tight co-design between array and PA / beamformer
  - Performance highly dependent upon trace losses and layout
Technical Challenges & Solutions
Essential Elements for a mmWave Technology

- High performance technology
  - High $f_T / f_{MAX}$ (3-5x operating frequency)

- Low loss BEOL
  - Cu backend, substrate resistivity

- Well-modeled technology
  - Good RF model-to-hardware correlation

- Design enablement
  - DRC/LVS/PEX

- Scalable transmission line & mmWave passives
  - Validated mmWave design library to minimize EM simulation
High Performance Technology

- $f_T / f_{MAX}$ should be 3 - 5x application frequency
- SiGe achieves both high $f_T$ and $f_{MAX}$
- CMOS $f_T$ continues to increase with scaling, but $f_{MAX}$ peaks at 65-40nm nodes due to $R_g \times C_{gd}$ product
- SOI seems to show most promise at advanced nodes in continuing to drive increased RF performance with reduced impact from $R_g \times C_{gd}$**

**Based on published data from multiple sources; multiple foundries included, but the data is not exhaustive. CMOS metrics are layout dependent (finger width, standard vs relaxed pitch, single vs. double gate contacts, number of contacts, metal levels, etc.)
Low Loss BEOL

Thin film transmission line with topside ground plane

Ground plane in BEOL prevents fields from entering substrate

Wavelength at 60GHz in SiO2 = 2.4mm; at 30GHz = 4.8mm
  • Long transmission lines not uncommon
  • Minimizing loss in BEOL is important

Availability of thick Cu levels and distance to ground planes are key to minimizing losses in BEOL
  • Distance to ground plane may be difficult to achieve in advanced nodes

mmWave modeling and scalable mmWave structures help reduce the design risk
Scalable Transmission Lines & mmWave Passives

- Microstrip and co-planar, single and coupled wires, with optional side shielding
- Full suite of microstrip discontinuities (mmWave passives)
- Scalable model / pcell: geometries and metal options
- Both time and frequency domain simulations

Skin effect circuit to capture high frequency effects

Excellent Model-to-E-M Field Solver Agreement
RF SOI for 5G
Why RF SOI?

Device stacking:
- Overcomes silicon Johnson Limit
- Improved efficiency vs. power combining

Substrate benefits for RF:
- Reduced parasitics $\rightarrow$ higher Q, lower loss and better noise figure
- Increased isolation/linearity

Logic and control integration:
- Potential for SOC integration

Low cost:
- Excellent balance between performance and integration

Mainstream silicon manufacturing:
- Readily available capacity

Source: FDSOI and RFSOI Forum – February 27, 2015
RF SOI for mmWave Applications

SOI has been extensively evaluated for mmWave building blocks:

- Measured peak $f_T$ is 264GHz for a 30 X 1007nm single-gate contact, relaxed-pitch transistor
- Best $f_{\text{MAX}}$ of 283GHz is achieved by a 58 X 513nm single-gate contact regular pitch transistor

RF SOI mmWave Power Amplifier Design

SOI enables transistor stacking for superior RF PA:
- Stacked configuration has higher power-added efficiency & smaller chip area vs. bulk CMOS:
  - Buried-oxide layer electrically isolates transistors, mitigating substrate leakage / breakdown
  - Configuration has higher input and output impedances for matching networks with lower loss & higher bandwidth
- Parasitic capacitances to substrate are significantly reduced, minimizing phase & voltage swing imbalance

Published results (45nm SOI):

<table>
<thead>
<tr>
<th>Source</th>
<th>Frequency range</th>
<th>PAE</th>
<th>Saturated output power</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>27 to 39GHz</td>
<td>33% @ 32GHz</td>
<td>22.4 dBm</td>
</tr>
<tr>
<td>2</td>
<td>25 to 35GHz</td>
<td>29% @ 29GHz</td>
<td>24.5 dBm</td>
</tr>
<tr>
<td>3</td>
<td>42 to 45GHz</td>
<td>34% @ 42.5 GHz</td>
<td>19.4 dBm</td>
</tr>
<tr>
<td>4</td>
<td>42 to 54GHz</td>
<td>42% @ 46GHz</td>
<td>22.4 dBm</td>
</tr>
</tbody>
</table>

1. “Millimeter-Wave Power Amplifiers in 45nm CMOS SOI Technology”, Jing-Hwa Chen, Sultan R. Helmi and Saeed Mohammadi
3. “A 34% PAE, 18.6dBm 42-45GHz Stacked Power Amplifier in 45nm SOI CMOS” Amir Agah, Hayg Dabag, Bassel Hanafi, Peter Asbeck, Lawrence Larson and James Buckwalter
4. “High-Efficiency Microwave and mm-Wave Stacked Cell CMOS SOI Power Amplifiers”, Sultan R. Helmi, Jing-Hwa Chen and Saeed Mohammadi, TMM 2015

Breaking High-Frequency Barriers in RF SOI

- Broadband frequency performance from 10MHz to 40GHz
- Highest linearity switch @ 40GHz
- Industry leading port-to-port isolation
- High reliability compared to GaAs & PIN alternatives (2KV HBM ESD)

Source: Peregrine supplied information
RF SOI mmWave RF Switch Design

RF SOI enables transistor stacking for superior RF switch performance:

- Buried-oxide layer electrically isolates transistors, mitigating substrate leakage
- Junction capacitors are much smaller
- Linearity is enhanced
- Optimizing for insertion loss is simpler
- 3-4 stack 45nm RFSOI switches are sufficient to meet the 24dBm power level with 25dBm isolation

Published results (45nm):

<table>
<thead>
<tr>
<th>Source</th>
<th>Frequency</th>
<th>Insertion Loss</th>
<th>Isolation</th>
<th>IIP3</th>
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<tbody>
<tr>
<td>1</td>
<td>45GHz</td>
<td>1.7 dB</td>
<td>&gt;25 dB</td>
<td>18.2 dBm</td>
</tr>
</tbody>
</table>

1. Source: M. Parlak, J.F. Buckwalter, "A 2.5-dB Insertion Loss, DC-60 GHz CMOS SPDT Switch in 45-nm SOI" CSICS 2011
RF SOI mmWave LNA Design

SOI enables cascode approach for superior RF LNA:

- Lower NF in cascode architecture (not possible in bulk Si)
- Enhanced stability due to lower parasitic capacitance
- Buried-oxide layer electrically isolates substrate, reducing noise coupling
- Linearity is enhanced

Published results (45nm):

Source: O. Inac, B. Getinoneri, M. Uzunkol, Y. A. Atesal and G. M. Rebeiz, “Millimeter-Wave and THz Circuits in 45-nm SOI CMOS”

Source: M. Parlak, J.F. Buckwalter, “A 2.5-dB Insertion Loss, DC-60 GHz CMOS SPDT Switch in 45-nm SOI” CSICS 2011
High Data Rate Sampling Converter Core in SOI

Dual channel high speed ADC for high data-rate communications & radar applications:

- 1024-bit CMOS output
- 42 to 68 GS/s conversion sampling rate
- 8-bit resolution
- Ultra-wide BW: 20GHz typical
- ± 0.8-bit differential nonlinearity
- ± 1.5-bit integral nonlinearity
- 5.8 bit ENOB to FS/4
- 0°C to +105°C Tj
- 2.3µ x 3.3µ core (32nm)

Source: Jariet datasheet, Rubicon-2 ADC macro
FD-SOI Body-Biasing Enables Power/Performance Trade-Off and Tuning of RF/Analog Parameters

- Forward Body Bias (FBB) enables low voltage operation without speed loss
- Reverse Body Bias (RBB) enables low leakage down to 1pA/micron
- Dynamic body biasing enables tuning RF/Analog characteristics: $g_M$, $g_{DS}$, self-gain, $f_T$, $f_{MAX}$
- Body biasing is an effective knob to tune RF performance characteristics

RF back gate bias reduces the $V_T$ and extends the dynamic range
RF SOI and the Road to 300mm

GLOBALFOUNDRIES is 1\textsuperscript{st} foundry to qualify and ramp a 300mm RF SOI technology into high-volume manufacturing:

- Long history of SOI manufacturing at 45nm and 32nm
- Development/ramp of customized RFSoI process (Peregrine UltraCMOS 11\textsuperscript{TM})

300mm RF SOI substrates provide benefits:

- Improved starting substrate uniformity
- Availability of stressor materials for lower Ron
- Availability of low-K materials for improved Coff

300mm RF SOI manufacturing provides advantages:

- Increased wafer productivity: \(~2.3\times\) over 200mm
- Improved edge yield for larger die sizes; reduced periphery over 200mm
- Reduced assembly cost per die; 10-15\% bump/CSP cost advantage per die compared to 200mm

Seamless transition to next generation RF processes:

- Creates learning on advanced tools which can be leveraged for next gen roadmaps
GLOBALFOUNDRIES RF Technology Offerings

Broadest portfolio in the industry focused on RF, μWave and mmWave!

<table>
<thead>
<tr>
<th>Technology</th>
<th>LOGIC</th>
<th>RFCMOS</th>
<th>SiGe PA</th>
<th>SiGe HP</th>
<th>RF SOI</th>
<th>HV &amp; PM</th>
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<td>45/40nm</td>
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- **Available**
- **In development**
- * FDSOI
- ** PDSOI
GLOBALFOUNDRIES
Worldwide Manufacturing and Support

- East Fishkill, New York
- Malta, New York
- Burlington, Vermont
- Dresden, Germany
- Singapore

5 manufacturing centers on 3 continents
* Localized technical support
Partnering for Success

Engagement
- Business development
- Product marketing
- Field sales

Development
- Field applications
- Technical support
- Process development
- PDK / modeling

Design & Front-end Services
- Foundational libraries & IP
- Third party design houses
- Alternative simulator support
- MPWs and prototyping

NPI & Manufacturing
- Customer engineering
- Reliability / failure analysis
- Skew lots and device “striping”
- Program management

Back-end Services
- Packaging: 2D / 2.5D / 3D
- Test
Summary

5G standards definition and requirements are continuing to evolve.

Millimeter wave operation for 5G poses both opportunities and challenges from a technology and design perspective...

Significant R&D has been done in evaluating the application of SOI to 5G architectures, with very positive results.

GLOBALFOUNDRIES is ready:

- Current thinking suggests millimeter wave spectrum may be in play
- Phased arrays and beamforming are enabling technologies to deliver on 5G promises
- SOI holds great promise in delivering on the key requirements of 5G systems
- Long history of SOI development and high-volume manufacturing, with a technology roadmap and support model aligned with the needs of the market & our customers
Thank you

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