Device performance driven by the substrate

**FD-SOI**

- 40,000 wafers @ ±1 Atomic layer
- Uniformity at all points on all wafers and at industrial level
- Excellent control of transistor geometry
- Key to fully depleted technologies

**RF-SOI**

- 300mm SOI ramp & 2nd gen RFesI
- HQF - 100 dBm
- IMD < -110 dBm
- IIP3 > 85 dBm
- Ron.Coff < 113 fs

**Technology roadmap**

- **Continue Moore's Law**
  - Si, strain Si, Ge or III-V
- **Long-term RF-SOI roadmap & solutions**
  - To integrate more RF functions

**Manufacturing capacity**

- **300mm SOI**
  - Up to 2M wafers/year capacity available when needed
- **200mm SOI**
  - > 1M wafers/year capacity available

**Partnership & collaboration to reach market needs**

- Soitec Bernin 2, France
- Pasir Ris, Singapore
- Simgui, China

- Quality system & certifications for automotive, consumer & industrial customers

- Other engineered substrates: Soitec power SOI, photonics SOI, imager SOI

- Soitec stacking for RF substrate
  - For devices with ultra-high linearity requirements

- Long-term roadmap for Soitec RFesI-SOI enhanced signal integrity substrate
  - For devices with high linearity requirements

- Design
  - Integrate smarter structures
- Process
  - Bring a smarter tool box
- Fabless
  - Develop the right device for the market
- Foundries
  - Develop the process based on SOI wafers
- Design, Process, Substrate, Fabless, Foundries: A comprehensive solution

Soitec, your innovation partner