FD-SOI In The Connected World

FD-SOI FORUM 2016, Tokyo

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Long History of Collaboration on FD-SOI

- Exploration on CPU/GPU designs with DC Explorer
  Sebastien PEURICHARD
  Choukri SAIDI
  STMicroelectronics
  June 10, 2014
  Grenoble, FRANCE

- Concurrent Top and Blocks Level Implementation of a High Performance Graphics Core
  Corine Pulvermuller
  Julien Guillemain
  STMicroelectronics
  June 11, 2013
  SNUG Grenoble

- FD-SOI Wide-Range DVFS Implementation with Synopsys Tools
  Frédéric NYER
  CPU Technical Lead
  Technology R&D / Central CAD & Design Solutions / CPU-GPU

- 28nm FD-SOI leakage optimisation with Synopsys Flow
  Pascal TEISSIER
  STMicroelectronics
  June 11th, 2013
  SNUG FRANCE

- Improving STA productivity at 32nm/28nmFD-SOI and below
  Sebastien Marchal
  STMicroelectronics
  June 10, 2014
  SNUG France

- In-Design Automatic DRC Repair Flow Using IC compiler and IC Validator
  Stephane Pautou
  STMicroelectronics
  June 10th, 2014
  SNUG Grenoble
Long History of Collaboration on FD-SOI

“.....it would have been exceedingly difficult to do a chip of this magnitude without IC Compiler II. "Our experience proved the promise we saw early in the design with 10X faster design exploration and 5X faster implementation, ...." 
- Thierry Bauchon, R&D Director, STMicroelectronics

“28-nm FD-SOI is an ideal solution for customers looking for extra performance and power efficiency ..... close collaboration with Synopsys and ST will enable designers to reduce risk, accelerate time-to-market, minimize power and maximize performance to expand 28nm FD-SOI .”
- Dr. Shawn Han, vice president of foundry marketing, Samsung Electronics
Galaxy Implementation Platform
Unified Solution of Best-in-Class Tools for Predictable Closure

Galaxy Design Platform
- RTL Synthesis
- Design Exploration
- Physical Guidance

QoR
- Signoff (STA and Extraction)

Area
- Standard Cell and Custom Co-design

Power
- PrimeTime
  - Design Compiler
  - IC Compiler I & II
  - IC Validator / StarRC

Closure
- Physical Design
  - In-design Physical Verification
  - HSPICE / CustomSim
  - Laker Layout
  - Custom Designer
Lynx Design System Accelerates TTM
Different Process Plug-ins to Target Different Capabilities

28 LPP

• Tech files and Libraries QA’d & configured
• Galaxy settings adjusted for 28LPP node:

```
SS28LPP.ARM.A {
    Bar via insertion settings
    sproc_source -file $SEV(techlib_dir)/tech/milkyway/cmos28lpp_BAR_7U1x_2T8x_LB.tcl
}
```

```
## SS28LPP settings
set_route_mode_options -route true
set_route_zrt_common_options -connect_within_pins {m1 via_wire_standard_cell_pins}
set_route_zrt_common_options -rotate_default_vias false
set_route_zrt_common_options -extra_nonpreferred_direction_wire_cost_multiplier \ 
    {m1 4} {m2 4} {m3 4} {m4 4} {m5 4} {m6 4} {m7 4} {m8 4} {m9 4}
set_route_zrt_detail_options -var_spacing_to_same_net true
```

28 FD-SOI

• Configured for vendor Tech Files and Libraries
• UPF driven body bias management across the flow
• UPF Supply set management for N-wells, P-wells and bias voltage control switch cells
• In-Design physical verification for bias connections
• Automated extraction & STA for additional corners at different body-bias points
• Analysis support for VC Static & Formal verification

• Quality results faster with starting point flows (CPU, GPU, DDR)
• Technology-specific scripts and settings
Synopsys Galaxy Design Platform
GLOBALFOUNDRIES 22FDX Enablement

- Full MV flow with UPF support for bias rails
- MCMM
- DMSA
  - PBA analysis
  - ECO leakage & timing fix
  - AOCV/POCV analysis
- In-design DRC checking
  - In-design Metal Fill
  - LVS
- Multi-rail extraction
  - Multi-valued SPEF
- DFT
  - Formal verification
  - Synthesis Placement Guidance
- Tapless cell library support
- Multi-rail routing
- CCD and CTS optimization flow
- Mixed-VTt spacing rule
- Non-uniform library FP
- Power mesh advanced flow
- DFM via kit (Redundant via)

Galaxy Design Platform
- Design Compiler
- Formality (RTL vs Gate Netlist)
- IC Compiler I & II
- Formality (Gate vs routed Netlists)
- IC Validator/StarRC
- PrimeTime
- Synopsys

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DesignWare IP Portfolio

- **ARC CPUs**: DDR PHY, DDR controller, PCIe PHY, PCIe controller, HDMI PHY, HDMI controller, USB PHY, USB controller, Ethernet controller, SATA PHY, SATA controller, MIPI PHY, MIPI controller, Bluetooth Radio, Bluetooth Link Layer, Security IP & SW
- **AMBA 4 AXI, AMBA 3 AXI & AMBA 2.0 AHB**: VIPs
- **AMBA APB**: VIPs
- **I2C, GPIO, UART**: I2C, GPIO, UART
- **Datapath & Floating Point**: Embedded Memories (SRAM, ROM, NVM)
- **Logic Libraries**: SD/eMMC controller

**Established Provider**
- ~$371M in Revenue
- Second Largest IP Vendor*

**Committed to Your Success**
- ~2,300 IP Engineers Worldwide

**Trusted IP Supplier**
- #1 in Interface, Analog, Embedded Memories, Physical IP

*Source: Gartner, March 2015

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DesignWare 28-nm FD-SOI IP Portfolio

With Interoperable Digital Controllers

**Analog IP**
- High speed PLLs
- ADC 10b & 12b 1MSps, sa.
- DAC 10b, video DAC
- DAC 24b, sigma delta audio

**Display IP**
- HDMI 1.4 PHY Tx v1.4
- HDMI 2.0 PHY Tx v2.0
- eDisplay Port PHY Tx v1.4
- Display Port 1.2 PHY Tx v1.2
- Combo HDMI/DP RX PHY

**Interface IP**
- USB 2.0 PHY
- USB 3.0 PHY
- DDR3/2 PHY
- LPDDR4 PHY
- PCIe 2.1 PHY
- PCIe 3.0 PHY
- XAUI PHY
- SATA PHY
- MIPI PHYs
Summary

• We are collaboration closely with partners help accelerate adoption of FD-SOI technology

• 28 FD-SOI – Ready today with tools, flow and IP

• 22FDX – Enablement for tools, flow underway
Thank You