Expanding FD-SOI Design and Application Options

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Outline

▲ VeriSilicon Overview
▲ FD-SOI Technology Benefit
▲ Benchmark Data
VeriSilicon’s Global Operations

- Founded in 2001, currently 673 (including Vivante) employees;
- 70% dedicated to R&D; 70% based in Shanghai, China;
- 70% of the revenue comes from outside of China.
VeriSilicon – A SiPaaS Company

**What we do**
- IP-centric
- Platform-based
- End-to-end turnkey service

**What we don’t do**
- No fab
- No branded product
  - No NRE investment
  - Limited inventory risk

We call it **Silicon Platform as a Service**, or **SiPaaS**
Diversified Customer Base for Growing End Markets

- Established Fabless and IDM Semiconductor Companies
- Emerging Fabless Semiconductor Companies
- OEMs ODMs
- Large Internet Platform Companies

VeriSilicon

- Consumer Electronics
- Mobility
- Wearables
- Networking

Note: Photographs reflect the general types of end products that can incorporate our solutions. We do not design or manufacture these end products.
From Specification to Tape-out to Shipment – End-to-end Service

- Tape out one chip a week; 50 chips a year
- 65% on advance technology nodes
- 98% first silicon success
IP-centric, Platform-based, End-to-end Turnkey Design Service

Revenue Categories

SoC Platforms

IP Portfolios

Note: Parenthesis indicate percentage of total revenue for the year ended December 31, 2013.
Strong Intellectual Property Portfolio

Over 1200+ Mix-Signal IC IPs driving Stickiness of Design Foundry Model

- **SOC infrastructure**
  - PLL / FPLL / SSPLL
  - OSC / POR / PRG
  - ADC / DAC
  - ......

- **Interface**
  - USB2.0 PHY
  - LVDS, CCP2
  - IQ ADC/ DAC
  - DDR, DUP IO
  - ......

- **HUI**
  - Audio Codec
  - Voice codec
  - Video codec
  - Touch screen
  - ......

- **Energy & Power**
  - HV current sensor
  - PMU
  - LDO
  - ......

- **Libraries & Memories**
  - General purpose
  - Customized cell & Mem
  - ......

180nm – 28nm

G or LL, LP, HV CMOS, COI, FD-SOI, half node, eFlash
Fully Depleted Transistors: FinFET and FD-SOI

Just a rotation ultimately converging when scaling BOX to TOX

FinFET
3D Fully Depleted Transistors

FD-SOI
2D Fully Depleted Transistors

Source: ST
Addressing Power Sensitive Markets

FinFet
- High end servers
- Laptops & tablet-PC

FD-SOI
- Consumer Multimedia
- Internet of Things, wearables
- Automotive

Source: ST
Samsung 28 nm FD-SOI vs. 28 nm HKMG/28 nm PSion

Performance @same leakage

Power @same speed

Chip Area

* Relative Comparisons

Source: Samsung
Samsung 28 nm FD-SOI Yield Ramp Up

Source: Samsung
VeriSilicon FD-SOI Task Force for three years

“White box” license of ST 28 nm FD-SOI IPs with modification rights

Source: ST
GF22FDX Introduction

- Industry’s first 22nm fully-depleted silicon-on-insulator (FD-SOI) technology
- Delivers FinFET-like performance and power-efficiency at 28nm cost
- Ultra-lower power consumption with 0.4 volt operation
- Software-controlled transistor body-biasing for flexible trade-off between performance and power
- Integrated RF for reduced system cost and back-gate feature to reduce RF power up to ~50%
- Enables applications across mobile, IoT and RF markets

- 70% lower power than 28HKMG
- 20% smaller die than 28nm bulk planar
- 20% lower die cost than 16/14nm
Forward Body-Bias (FBB) extends FD-SOI flexibility

- 50% lower power at same frequency
- 40% faster performance at same power
- Low Vdd operation (down to 0.4 volts)
- FBB Advantage: Software-controlled body-bias enables dynamic tradeoffs between power, performance and leakage
Body-biasing Enables Power/Performance Trade-off
Body-bias allows for optimum power/performance trade-off
GF22FDX vs GF28SLP vs GF28HPP

- 9 stages of RO, with FO3, TT/25c
- 22FDX @ 0.7v can achieve the same performance as 28SLP @ 1.0v
- Dynamic power on 22FDX is 65% of its on 28HPP, and it’s 36% of its on 28SLP

- Leakage power on 22FDX is 50% of its on 28SLP, and 25% of its on 28HPP
Memory (2Kx72) @ 800MHz on 22FDX

- Target speed @ 800MHz
- HC124 core cell @ 0.8v
- Memory periphery has its independent Vdd and bias voltages (Vbn/Vbp/Vbcorecell)
- SLVT @0.55v with 2v/-2v/1.8v has the lowest active power and total power, even though the leakage is the highest due to FBB and SLVT
ARM Cortex-A7 is one of the most popular processors, from low-end to high-end. Different A7 cases help us evaluate the Power/Performance/Area on different process nodes.

- **800Mhz** Low-end application
  - GF28SLP / GF22FDX

- **1.2Ghz** Mid-end application
  - GF28HPP / GF22FDX / GF14FF LPP

- **Super Low Voltage 0.4V**
  - GF28SLP / GF22FDX
**Process Exploration on Cortex-A7 @ 800Mhz**

**Observations**

- With 8T library, GF22FDX is 50% lower in area/dynamic power compared with GF28SLP
- Main stream, middle level performance, cost sensitive applications -> GF22FDX

- Performance @ 800Mhz_SS_n40C
- Leakage/Dynamic power @ TT_25C
- GF28SLP: RVT+LVT, VDD = 1.0v
  - GF22FDX: 8T LVT, VDD = 0.80v (without BB)

**Leakage Power**

<table>
<thead>
<tr>
<th></th>
<th>GF28SLP</th>
<th>GF22FDX 8T LVT no BB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>1.00</td>
<td>1.01</td>
</tr>
</tbody>
</table>

**Dynamic Power**

<table>
<thead>
<tr>
<th></th>
<th>GF28SLP</th>
<th>GF22FDX 8T LVT no BB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>1.00</td>
<td>0.52</td>
</tr>
</tbody>
</table>

**Area**

<table>
<thead>
<tr>
<th></th>
<th>GF28SLP</th>
<th>GF22FDX 8T LVT no BB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>1.00</td>
<td>0.49</td>
</tr>
</tbody>
</table>
Process Exploration on Cortex-A7 @ 1.2Ghz

Observations

▲ For Cortex-A7 performance exceeding 800MHZ, GF28HPP can achieve but...
▲ Using GF22FDX 12T library is more power and area efficient!
  ▼ GF14FFLPP exceeds GF22FDX in PPA but much more expensive
  ▼ GF22FDX can be very close to GF14FFLPP with Leakage/Dynamic power if using 12T library, with a little bigger area compared with 8T library
▲ Mainstream, middle level performance, cost sensitive applications -> GF22FDX
▲ Higher performance applications -> GF14FFLPP

▲ Performance @ 1.2Ghz_SS_n40C
▲ Leakage/Dynamic power @ TT_25C

<table>
<thead>
<tr>
<th></th>
<th>Leakage Power</th>
<th>Dynamic Power</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>GF28HPP</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>GF22FDX 8T noBB LVT+sLVT</td>
<td>0.49</td>
<td>0.77</td>
<td>0.50</td>
</tr>
<tr>
<td>GF22FDX 12T FBB0v/-1v LVT</td>
<td>0.20</td>
<td>0.72</td>
<td>0.59</td>
</tr>
<tr>
<td>GF14 FF LPP</td>
<td>0.16</td>
<td>0.71</td>
<td>0.29</td>
</tr>
</tbody>
</table>

▲ GF28HPP: RVT+LVT, VDD = 0.85v
GF22FDX: 8T LVT+sLVT, VDD = 0.80v (without BB)
GF22FDX: 12T LVT, FBB 0v/-1v VDD = 0.80v
GF14FF: RVT+LVT, VDD = 0.80v
**Process Exploration on Cortex-A7 based on 12T**

**Observations**

▲ Body-Bias & Vth options are flexible knobs which can help GF22FDX 12 T library to cover application use cases ranging from 800MHZ – 2.0GHZ, with some area penalty.
▲ Leakage is processed by logarithm, it plays more roles in higher performance applications, due to higher FBB and SLVT
▲ 1.8GHZ~2GHZ can be a high limit for GF22FDX 12T library when power starts to increase dramatically

*The data are processed by normalization based on 800Mhz case.*
### Observations

▲ **Power efficiency is another indication of FD-SOI technology value**

\[
\text{Total Power Eff} = \frac{\text{Total Power}}{\text{Freq}}
\]

\[
\text{Dynamic Power Eff} = \frac{\text{Dyn Power}}{\text{Freq}}
\]

▲ **Lower Vdd supply for logic operation is key value of FDSOI**

▲ **Performance @ 800/500/200Mhz_SS_n40C**

▲ **Leakage/Dynamic power @ TT_25C**

▲ **GF28SLP:** RVT+LVT, VDD = 1.0v

▲ **GF22FDX:** sLVT, VDD = 0.4v (with 1v/-2v FBB)

<table>
<thead>
<tr>
<th></th>
<th>Total Power Eff</th>
<th>Dynamic Power Eff</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GF28SLP 0.9v@800Mhz</strong></td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td><strong>GF22FDX 0.4v@500Mhz</strong></td>
<td>0.31</td>
<td>0.16</td>
<td>0.55</td>
</tr>
<tr>
<td><strong>GF22FDX 0.4v@200Mhz</strong></td>
<td>0.30</td>
<td>0.14</td>
<td>0.49</td>
</tr>
<tr>
<td><strong>GF28SLP 0.9v@800Mhz</strong></td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td><strong>GF22FDX 0.4v@500Mhz</strong></td>
<td>0.16</td>
<td>0.14</td>
<td>0.55</td>
</tr>
<tr>
<td><strong>GF22FDX 0.4v@200Mhz</strong></td>
<td>0.14</td>
<td>0.14</td>
<td>0.49</td>
</tr>
</tbody>
</table>
Status and Future Work

▲ 28nm FD-SOI
  ► The technology and ecosystem is mature
  ► Customer design wins
    ■ Graphics processor application
    ■ Network application

▲ 22nm FD-SOI
  ► Continuing benchmark on A7/M0/Memory/Device based on PDK 0.4
  ► Silicon validation on MPW of analog/RF test structures in March 2016
  ► Complex IP MPW on June 30th 2016
  ► VeriSilicon IoT platform is to be designed on GF22FDX
    ■ Expecting a 9T 0.6v library supporting 6 layers metal, targeting for IoT and low power application, which will be released by mid of Feb 2016