Mixed-Signal Design Innovations in FDSOI Technology

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Outline

- Application trends and needs
- Review of FDSOI advantages
- Examples
  - High-speed data conversion
  - RF transceivers
  - Medical imaging
  - Machine learning
The Big Picture

- Various terminology for the same overarching trend
  - Third paradigm
  - Ubiquitous computing
  - Internet of Everything

Hardware Platforms → Physical World

Software, Networks → Virtual World

Fusion of Physical and Virtual Worlds
The Big Picture

1. Smart Objects
2. Networks
3. Insights

Sense
Act

Sophie V. Vandebroek, Three Pillars Enabling the Internet of Everything, ISSCC 2016 Keynote Talk
Implications

- Unprecedented opportunities for new businesses
- New forms of human-machine interaction
  - Virtual reality, wearable devices, …
- New kinds of sensors, actuators
  - Medical diagnostics, robotics, …
- Fundamental change in the nature and volume of data
  - Vast amounts of data at the “edge” requiring local processing
  - Cloud computing ↔ fog computing
Selected Needs in Mixed-Signal/RF Design

- Ultra low-power analog interfaces
- Ultra low-power fog computing
- Universal radios
- Ultra high-speed, low energy data links
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Variability

- Tighter process corners and less random mismatch than bulk processes

- Benefits
  - Simpler design process, shorter design cycle
  - Improved yield or improved performance at given yield

[Le Tual, ISSCC 2014]
Switch Performance

- Improved gate control allows for small $V_{TH}$
- Backgate bias allows for additional $V_{TH}$ reduction on demand
- Result is an unprecedented quality of analog switches
- Key for high-performance data converters and other SC circuits
- Compounding benefits:
  - Smaller $R$ → Smaller switch → Compact layout → Lower parasitics → Even smaller switch

[Le Tual, ISSCC 2014]
Reduced Junction Capacitance

- Low $C_j$ makes a substantial difference in high-speed design
  - Drastic reduction of self-loading in gain stages
  - Drastic reduction of switch self-loading

- This not only leads to incremental improvements, but allows the designer the use circuit architectures that would be infeasible/inefficient in bulk technology
  - Some examples to follow
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Increasing Need for Bandwidth

- Core Networking Doubling = 18 mos
- Gigabit Ethernet
- 10 Gigabit Ethernet
- 40 Gigabit Ethernet
- 100 Gigabit Ethernet

Date:

Motivation – Increasingly Complex Modulation

- Both electrical and optical systems are trending away from simple NRZ signaling
- Requires linear front-end circuits and very high-speed A/D converters

Reference: K. Roberts et al., IEEE Communications Magazine, July 2010
ADC Landscape in 2005

Data: http://web.stanford.edu/~murmann/adcsurvey.html

\[ FOM_W = \frac{P}{f_s \cdot 2^{\text{ENOB}}} \] at \( f_{\text{in}} \approx \frac{f_s}{2} \)
ADC Landscape in 2010

Data: http://web.stanford.edu/~murmann/adcsurvey.html
ADC Landscape in 2015

Data: http://web.stanford.edu/~murmann/adcsurvey.html
ADC Landscape in 2015

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○ 28 FDSOI or 32 SOI
State of the Art: 8b, 90 GS/s, 667 mW

<table>
<thead>
<tr>
<th>Technology</th>
<th>32nm SOI CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>TI-SAR</td>
</tr>
<tr>
<td>Resolution</td>
<td>8</td>
</tr>
<tr>
<td>Sampling speed (GHz)</td>
<td>70 80 90 100</td>
</tr>
<tr>
<td>Supply $V_{DA}/V_{DI}$ (V)</td>
<td>1.0/1.1 1.1 1.2 1.27</td>
</tr>
<tr>
<td>Input range ($V_{pp-diff}$)</td>
<td>0.7 0.7 0.8 0.85</td>
</tr>
<tr>
<td>SNDR (0-6.1GHz) (dB)</td>
<td>37.7 37.2 36.0 34.9</td>
</tr>
<tr>
<td>SNDR (0-19.9GHz) (dB)</td>
<td>34.2 32.9 33.0 27.7</td>
</tr>
<tr>
<td>3dB bandwidth (GHz)</td>
<td>22</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>355 477 667 845</td>
</tr>
<tr>
<td>FOM (0-6.1GHz) (fJ/conv. step)</td>
<td>81 101 144 186</td>
</tr>
<tr>
<td>FOM (0-19.9GHz) (fJ/conv. step)</td>
<td>121 165 203 426</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.45</td>
</tr>
</tbody>
</table>

Reference: Kull et al., ISSCC 2014
Two switches in series
→ Takes advantage of SOI

Reference: Kull et al., ISSCC 2014
RF Goes Switch-Cap → Universal Radios?

- Paradigm shift toward translational circuits, N-path filters
- Enabled by switch performance in modern CMOS technology
- FDSOI provides same advantages as seen in the data converter examples

Ultrasound Goes Handheld and Wearable

A. Bhuyan

*Verasonics Imaging System*

*CMUT Probe*

*Butterfly Network*

*Source (bottom): http://www.ultrasoundschoolsinfo.com/next-wave-ultrasound-technology/*
Work in Progress: Integrated Ultrasound Receiver

Ultrasound transducer

CMUTs

Densely Integrated Rx (USRX)

Package

Content removed
Work in Progress: Integrated Ultrasound Receiver

Content removed
Area of State-of-the-Art $\Delta \Sigma$ Modulators

BW=5MHz~25MHz, and SNDR=50dB~75dB

- SDCT(ISSCC)
- SDCT(VLSI)
- SDSC(ISSCC)
- SDSC(VLSI)


This $\Delta \Sigma$
28nm FDSOI

Power [W]

Area [mm$^2$]

Pixel area
Example: Image Classification

- Many interesting problems to solve
- Wide range of algorithms and complexity

Sources: Choi, ISSCC 2015; Stanford CS231; D. Hammerstrom
ImageNet Large Scale Visual Recognition Challenge

http://image-net.org

Workhorse of Contemporary Machine Learning:
Convolutional Neural Network

Modern Deep CNN: 5 – 152 Layers

Are We Ready?

State-of-the Art Custom Hardware

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>NVIDIA TK1 (Jetson Kit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm</td>
<td>28nm</td>
</tr>
<tr>
<td>Clock Rate</td>
<td>200MHz</td>
<td>852MHz</td>
</tr>
<tr>
<td># Multipliers</td>
<td>168</td>
<td>192</td>
</tr>
<tr>
<td>On-Chip Storage</td>
<td>Buffer: 108KB Spad: 75.3KB</td>
<td>Shared Mem: 64KB Reg File: 256KB</td>
</tr>
<tr>
<td>Word Bit-Width</td>
<td>16b Fixed</td>
<td>32b Float</td>
</tr>
<tr>
<td>Throughput</td>
<td>34.7 fps</td>
<td>68 fps</td>
</tr>
<tr>
<td>Measured Power</td>
<td>278 mW</td>
<td>Idle/Active²: 3.7W/10.2W</td>
</tr>
<tr>
<td>DRAM Bandwidth</td>
<td>127 MB/s</td>
<td>1120 MB/s</td>
</tr>
</tbody>
</table>

1. AlexNet Convolutional Layers Only
2. Board Power
3. Modeled from [Tan, SC11]

Digital Multiplier
Motivation for Mixed-Signal Compute

![Graph showing power costs between digital and analog systems.](image)

Limit set by 1/f noise for a fixed area consumption.

R. Sarpeshkar, Analog Versus Digital: Extrapolating from Electronics to Neurobiology
Charge Domain Dot Product Kernel

- Externally digital, internally analog compute block
- Amenable for digital CMOS VLSI integration
- ADC energy amortized over several multipliers
- Multiply via multi-phase charge redistribution
- Add via passive charge sharing among multipliers
- Small unit caps < 1fF
- Expecting total energy of ~2pJ for 16x8b MAC

*Murmann, Bankman, et al., Asilomar 2015*
Example: 12 x 9

\[ Q_W = 12C_u V_{ref} \]

\[ V_W = \frac{12}{15} V_{ref} \]

\[ Q_{WX} = \frac{12}{15} V_{ref} \cdot 9C_u \]

\[ V_{WX} = \frac{12}{15} \cdot \frac{9}{15} V_{ref} \]

Summary

- The transition to the “third paradigm” brings interesting opportunities and challenges
  - Mixed-signal IC design is no exception

- FDSOI technology offers significant benefits toward addressing the resulting needs
  - Ultra low-power fog computing
  - Densely integrated, low-power analog interfaces
  - Universal radios
  - Ultra high-speed ADCs
  - …
Questions?