SMART TECHNOLOGY CHOICES AND LEADERSHIP I.MX APPLICATIONS PROCESSORS

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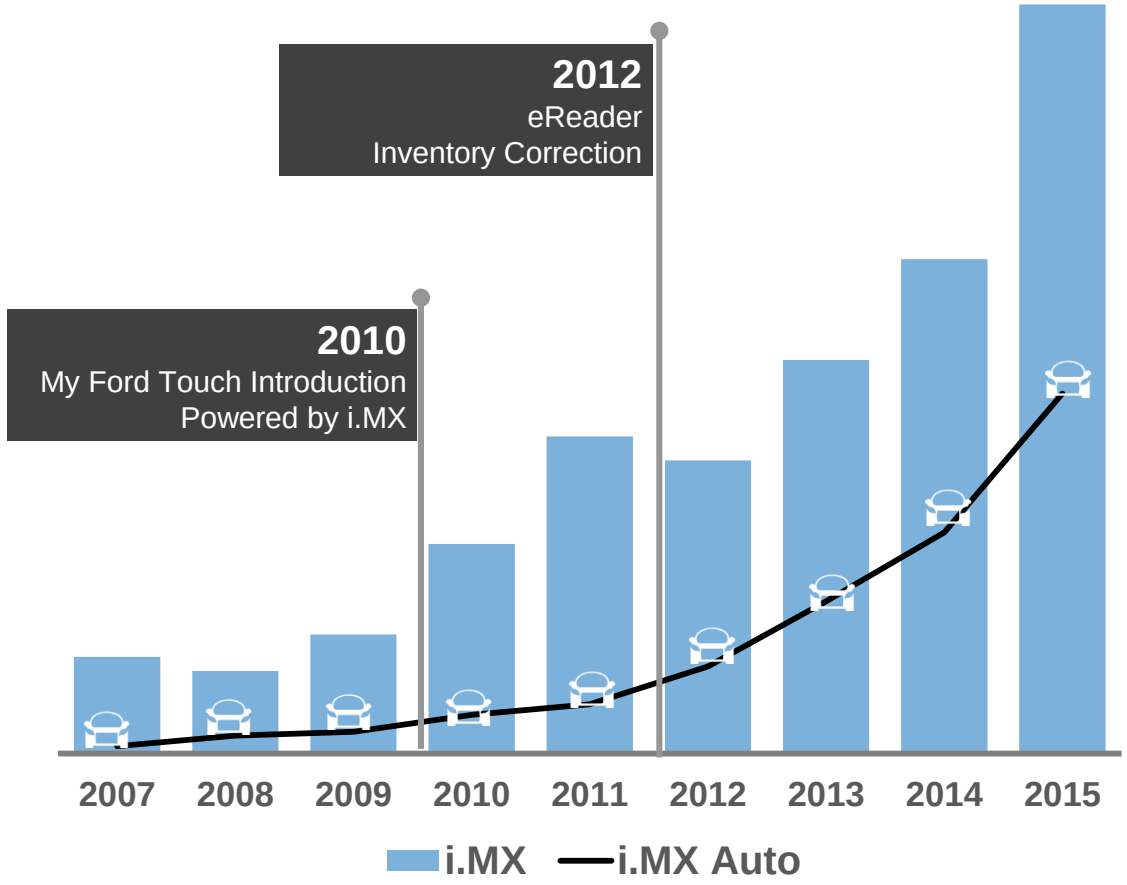
SECURE CONNECTIONS FOR A SMARTER WORLD

Smart World – Secure, Connected, Low-Power, Scalable

i.MX Driving Explosive Growth in Smart Vehicles & Smart Devices



Over 200M i.MX SOCs shipped to date

Over 35M vehicles enabled with i.MX since 2007

Leader in eReaders and Auto Infotainment MPU

i.MX 6 Series: Supreme Scalability and Flexibility
Leverage One Design into Diverse Product Portfolio

Scalable series of **NINE** ARM-based SoC Families

i.MX 6UltraLite Family	i.MX 6SoloLite Family	i.MX 6SoloX Family	i.MX 6Solo Family	i.MX 6DualLite Family	i.MX 6Dual Family	i.MX 6DualPlus Family	i.MX 6Quad Family	i.MX 6QuadPlus Family

Pin-to-pin Compatible

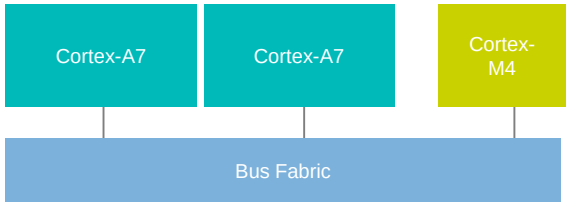
Software Compatible

Expanded series for performance, power efficiency and lower BOM

Recently Announced i.MX 7D & 7S Advantages

Advanced Heterogeneous Architecture

- Single and Dual Cortex-A7 Core up to 1GHz
- Cortex-M4 up to 266MHz
- Offload Tasks
- Optimize Power
- Increase Security



Unmatched Power Efficiency

- 3x improvement in Power Efficiency vs i.MX 6
- 100 uW/MHz for Cortex-A7
- 70 uW/MHz for Cortex-M4
- One third the power consumed in the Low Power suspend mode (250uW) vs i.MX 6

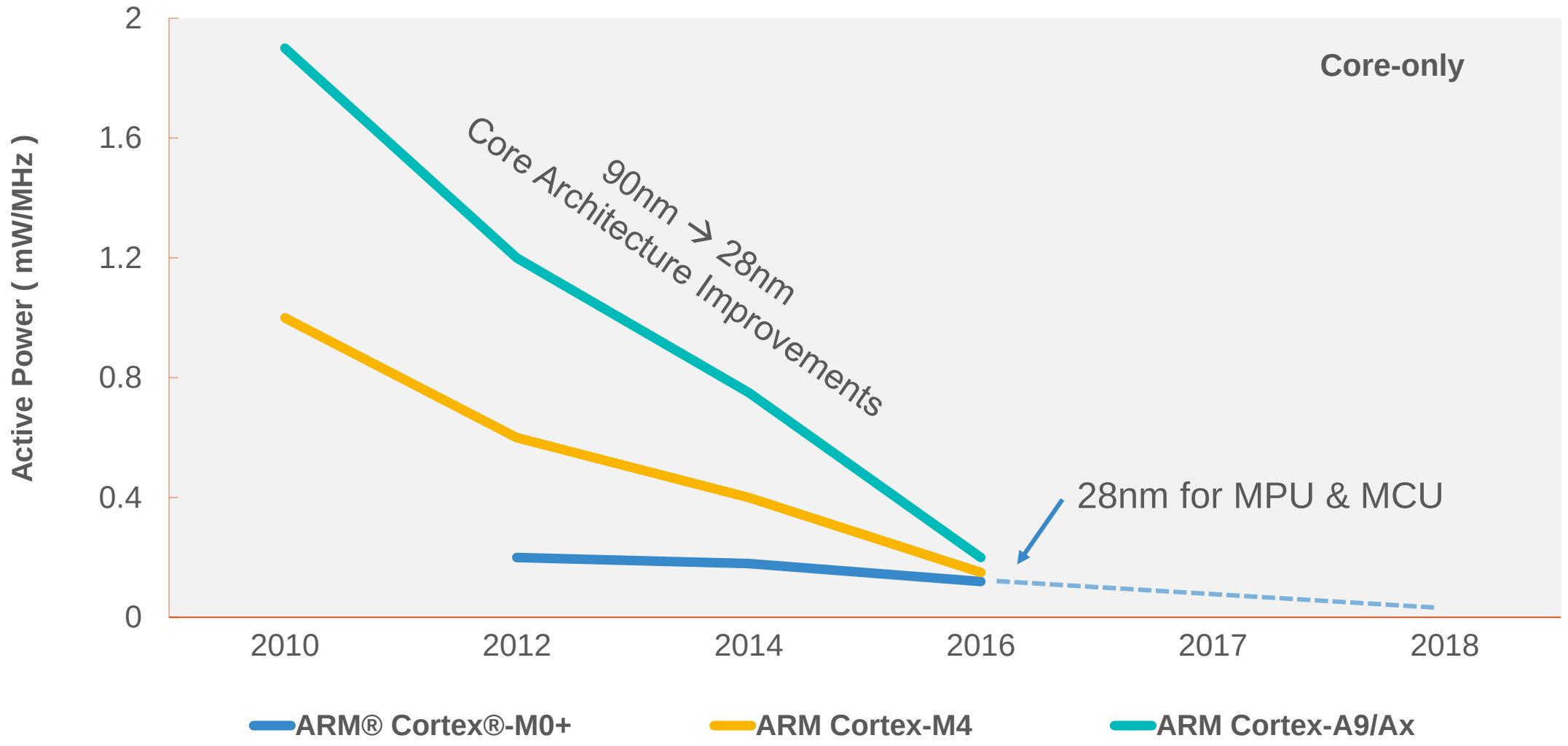
Enabling Flexible High Speed Connectivity

- PCI-e v2.1
- Dual Gbit Ethernet with AVB
- DDR QuadSPI support
- eMMC 5.0

Complete Security Infrastructure

- Secure Boot
- Crypto H/W Acceleration
- Internal and External Tamper Detection
- Secure RAM
- DPA attack Resistance
- Secure JTAG

Processing Power Efficiency



i.MX Processor Roadmap

Two New i.MX Platforms Based on 28nm FD SOI Technology

i.MX 6 QuadPlus

↓

i.MX 6 Quad

↓

i.MX 6 DualPlus

↓

i.MX 6 Dual

↓

i.MX 6 DualLite

↓

i.MX 6 Solo

↓

i.MX 6 SoloX

↓

i.MX 6 SoloLite

↓

i.MX 6 UltraLite

ARM® v7-A

i.MX 8 series

Advanced Graphics & Performance

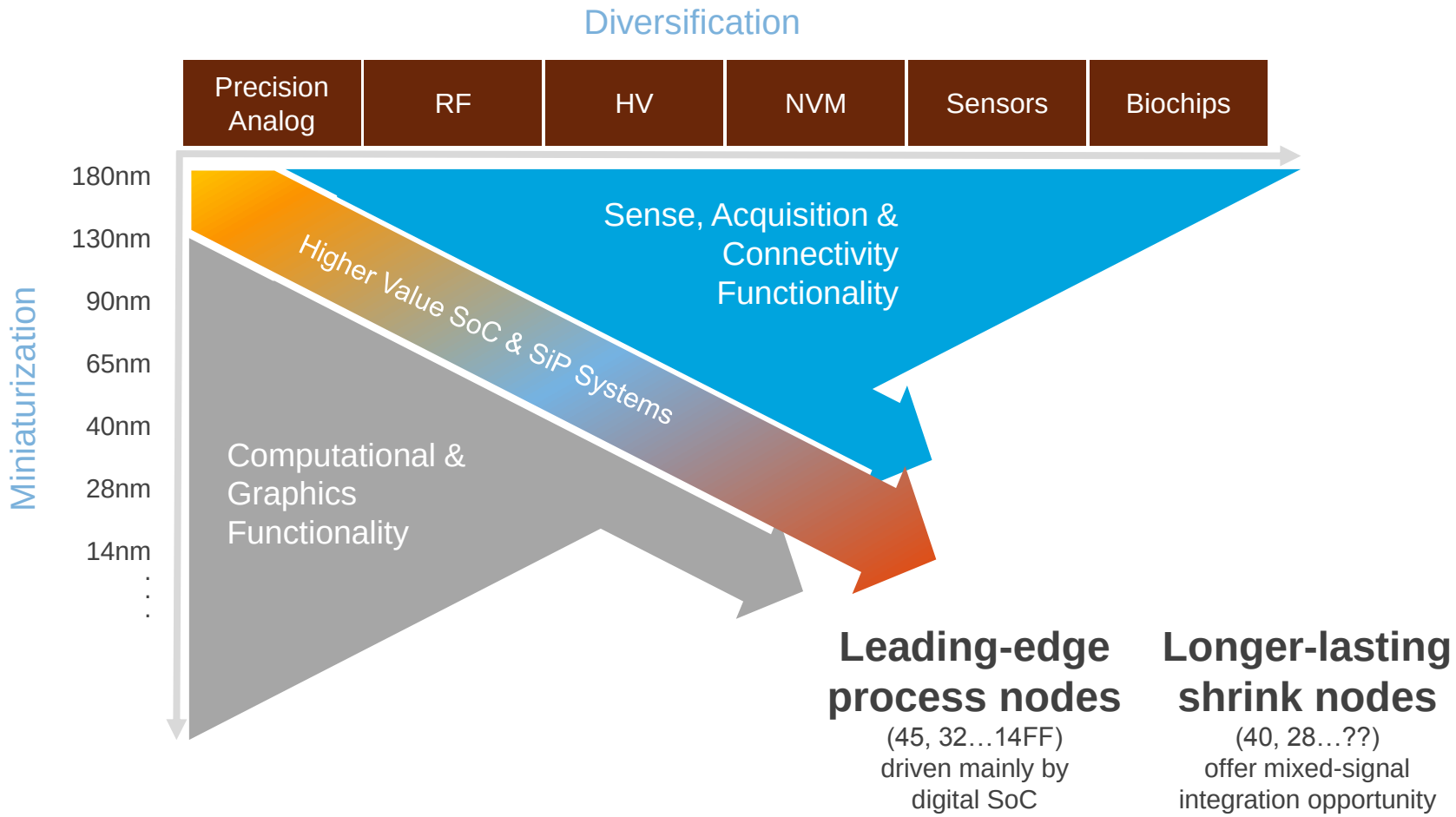
ARM ® v8-A

i.MX 7 series

Power Efficiency

ARM® v7-A

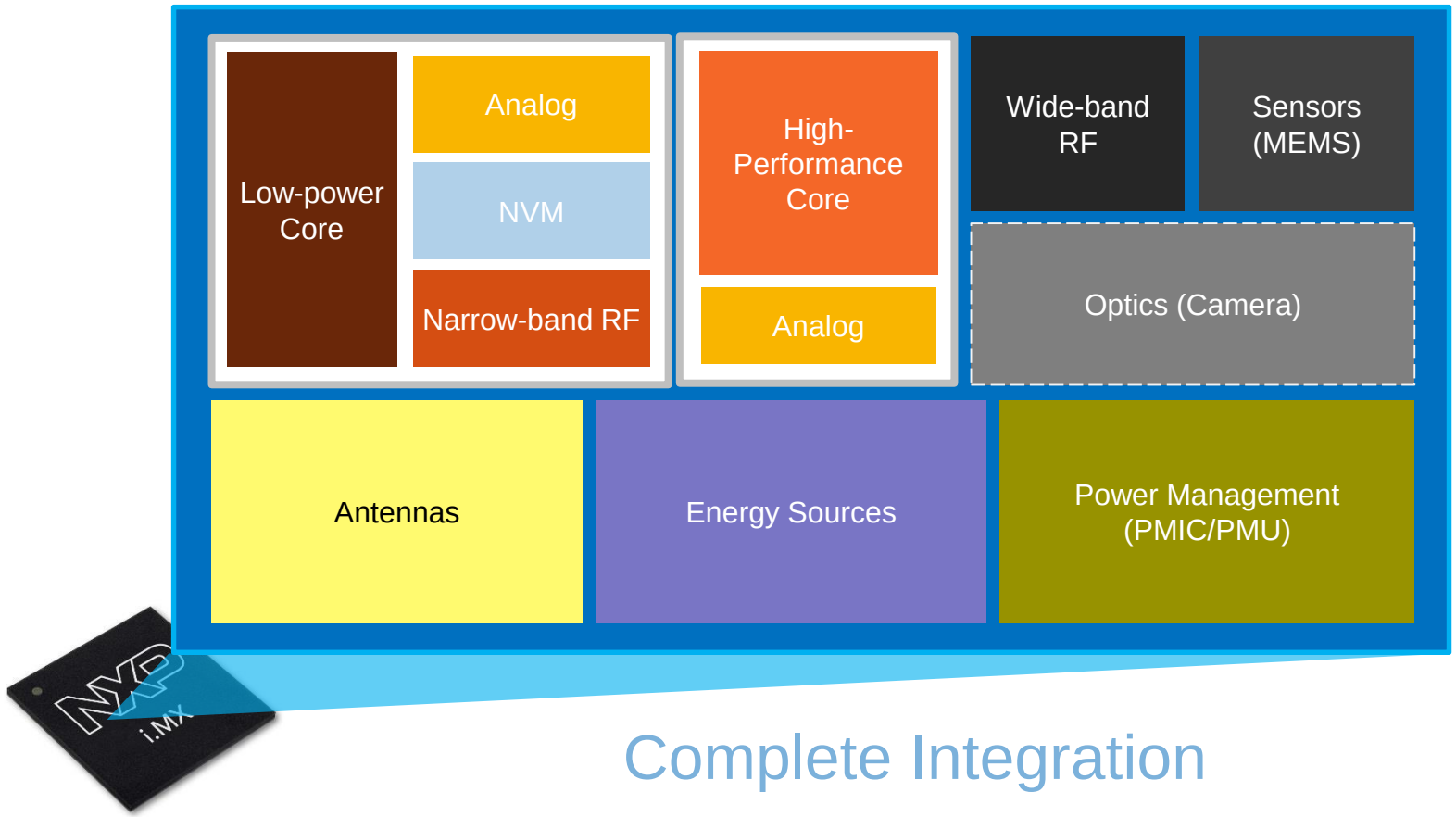
Increasing Integration of Diverse Components



Leading-edge process nodes
(45, 32…14FF)
driven mainly by digital SoC

Longer-lasting shrink nodes
(40, 28…??)
offer mixed-signal integration opportunity

End Nodes of TOMORROW

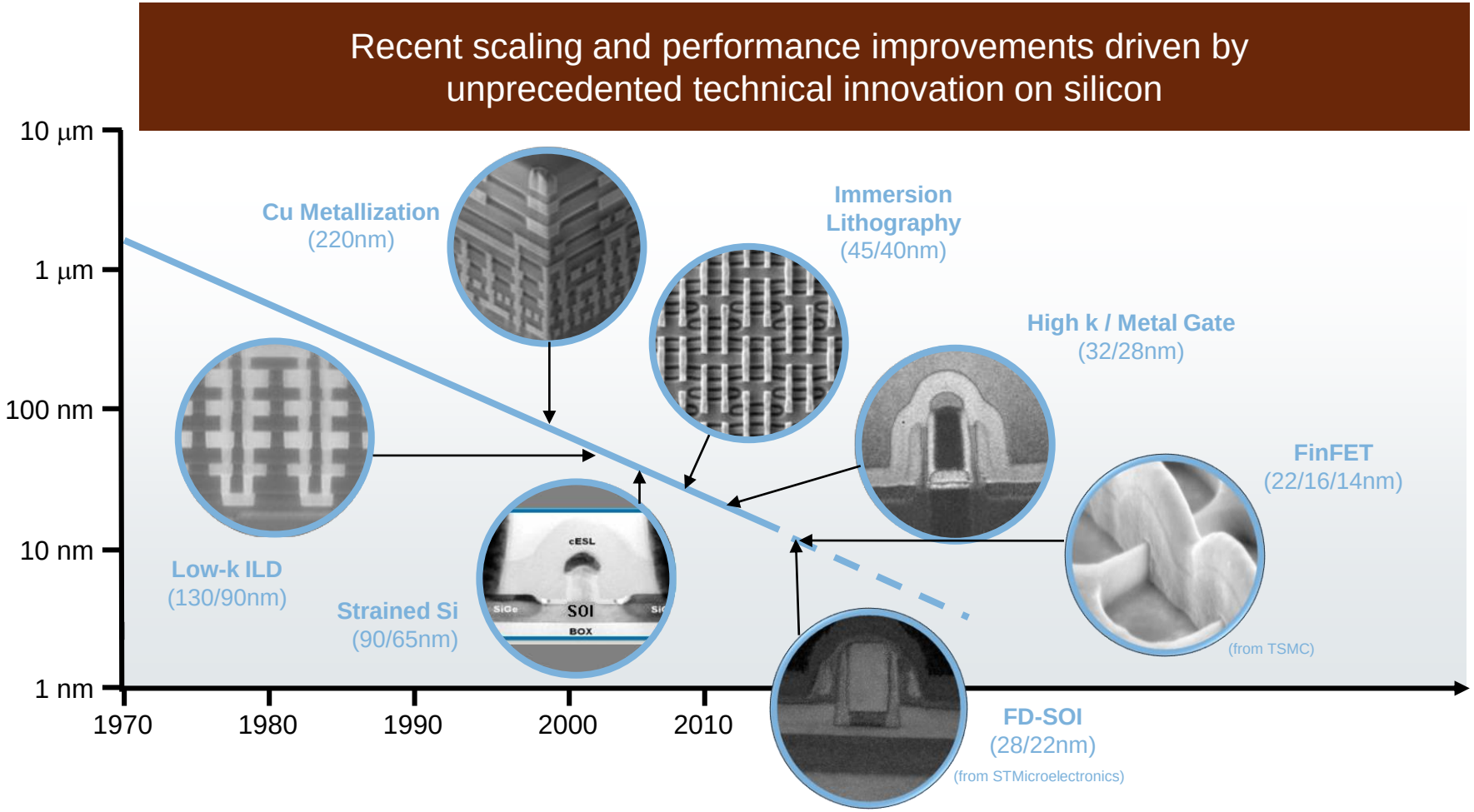


Complete Integration

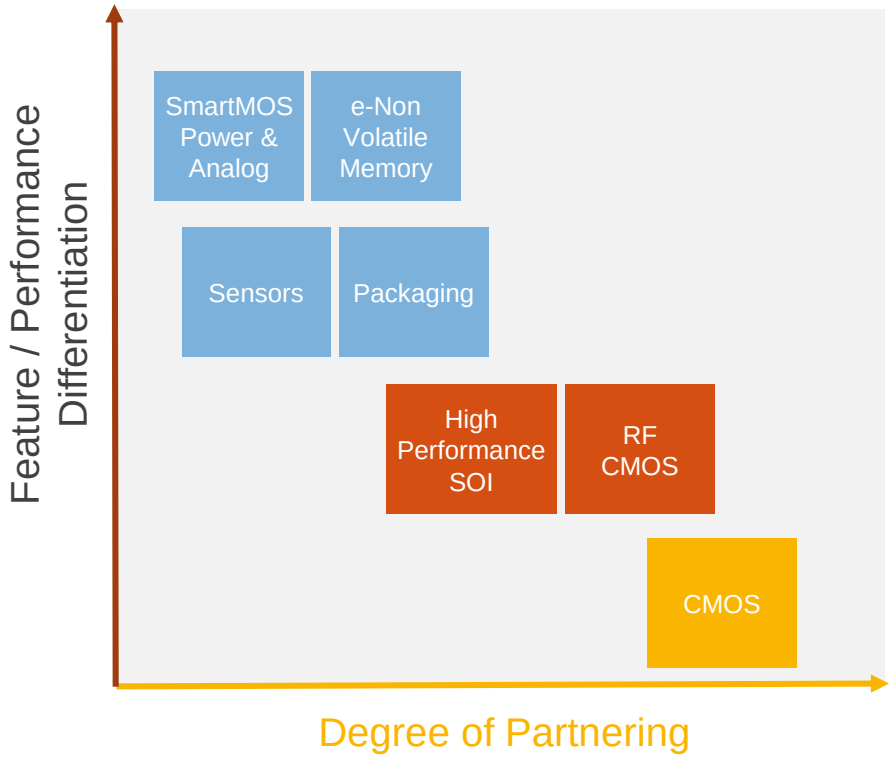
Scaled and all-in-one small, thin form factor package

Moore's Law

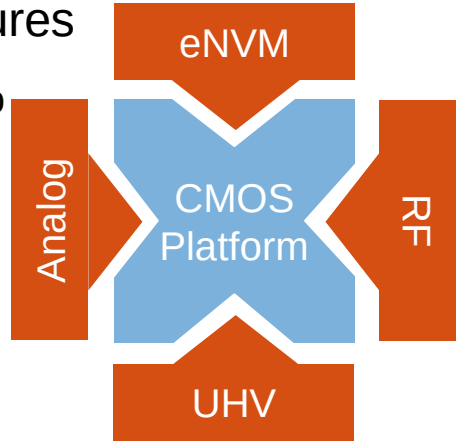
"No Exponential is Forever…but Forever can be Delayed"



NXP Process Development Strategy



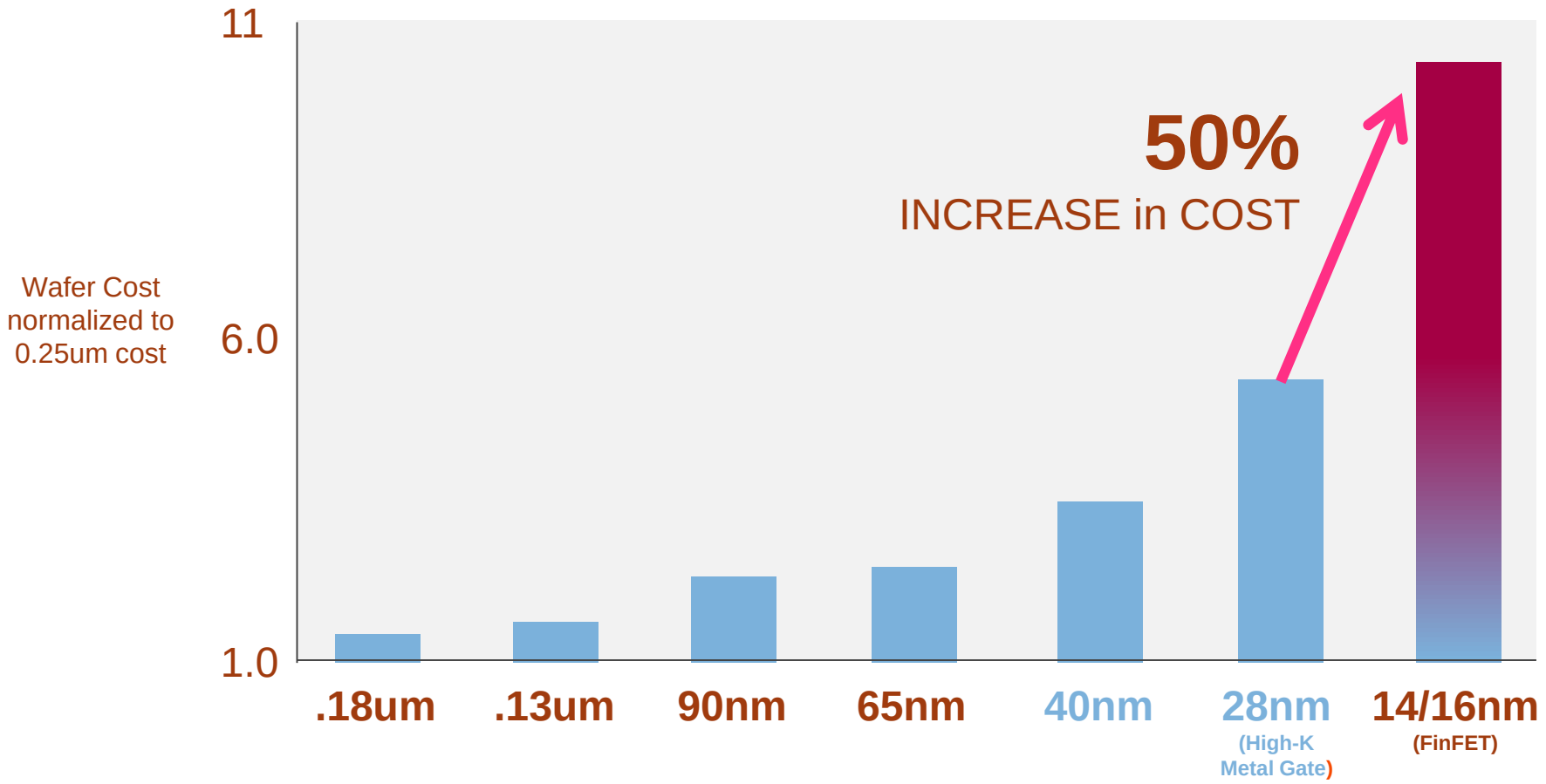
- **CMOS Platform-Based Technologies:**
  - Leverage foundry standard technology
  - Adapt for targeted applications
- **Differentiating Technologies:**
  - Focus on performance/features
  - High re-use >80% of the technology platform
  - Wholly-owned intellectual property



Smart Technology Choices

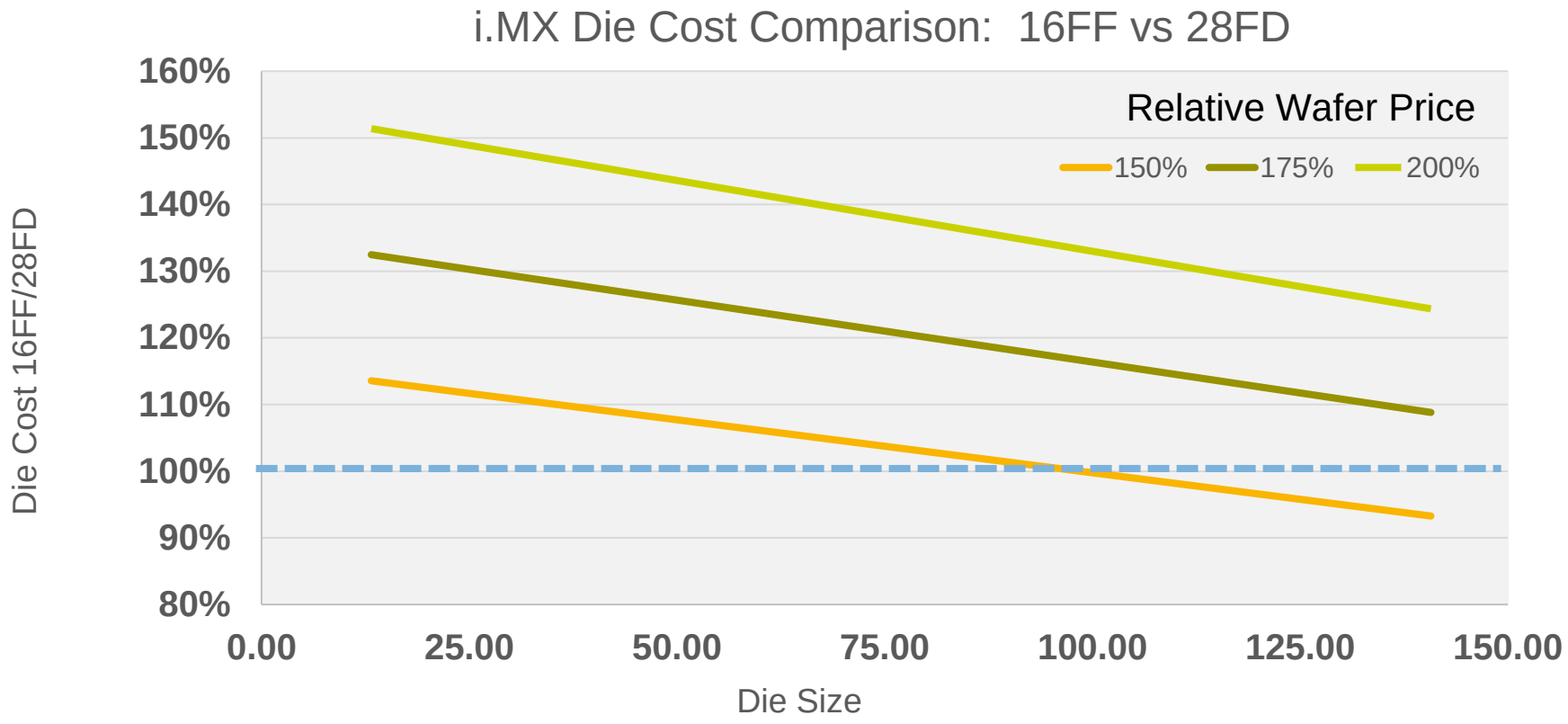
1. Which node?
2. Which process architecture?

28nm – ‘Last Simple Node?’



40nm to 28nm will be significant % of worldwide capacity in 2020

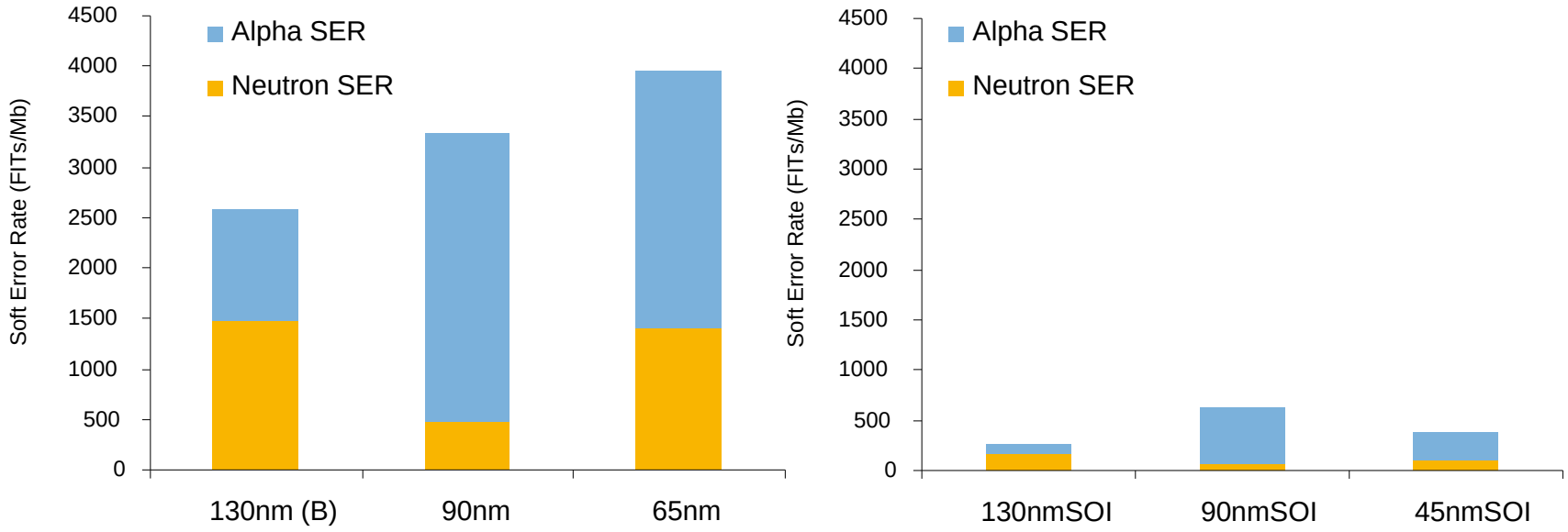
Cost Vs. Performance



i.MX Processors

- Large range of die size
- Larger amount of analog
- Pads and overhead not scaling
- Future RF integration

NXP History Leveraging SOI



- NXP has developed 20+ processors over 3 generations of SOI technology
- Soft Error Rate (SER) is becoming an increasingly significant factor as SoC memory arrays continue to increase in size & density
- Bulk technology performs successively worse with each technology node
- SOI provides 5 ~ 10x better SER reliability and the gap is widening as geometries shrink
- 28 FD SOI benefits extend to 10-100X better immunity

SER Comparison

Technology	Intrinsic (Technology) SER	Product-Level SER
28nm Bulk Si	Moderate	Design techniques / protection
28nm FD-SOI	Low	Protection techniques depend on amount of memory and logic content
14/16nm FinFET	Low	Protection techniques depend on amount of memory and logic content

FD SOI Advantages

1

Power-Performance Benefits

Low Vdd with Performance
Improved Electrostatics
Scalable Platform

2

Analog & RF Characteristics

Better Gain, Matching, Noise
Gate 1st Integration

3

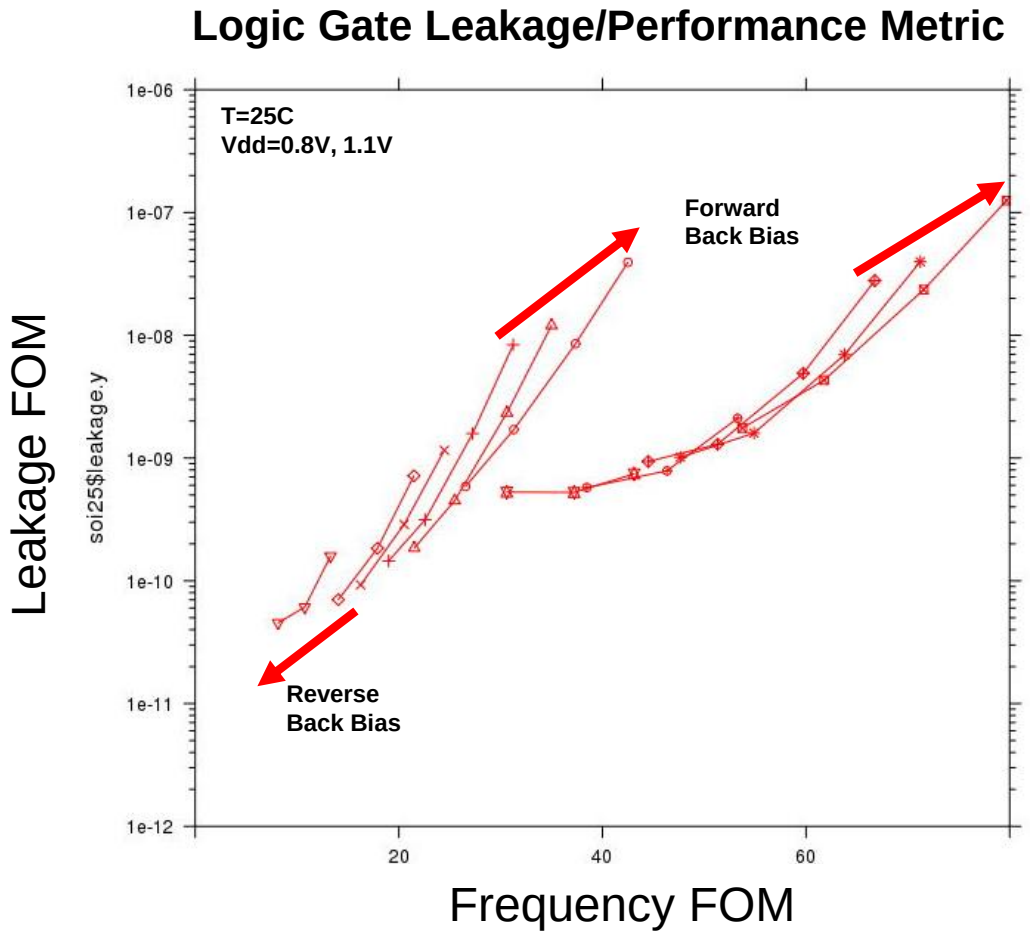
Lower Risk Manufacturing

Simple Integration / Fast TAT
Extends 28nm install base
Low complexity planar device

28nm FD-SOI Platform

Back-bias enables large dynamic operating range

Good power-performance at low voltages, temperatures (IOT standby mode)



Each point represents simulated average over three X1 library cells from a unique Vt-L combination. Ignores interconnect impact, which is highly implementation dependent

Process Technology Implications

28nm & Beyond	High-K Metal Gate	FD-SOI	FinFET
Energy Efficiency			
Cost Competitiveness			
Ease of Design			
Ease of Diversification			

Multi-Cores

- Power Management
- Performance
- Security / ARM® TrustZone

Memory

- Secure Java / OS support
- Connectivity S/W stack

Non-volatile Memory

- Program Complexity
- Data Collection

RF Connectivity

- Wireless Everywhere

FD SOI Gaps Addressed by NXP

1

Utilizing Full Range of Back-Gate Biasing

Extended Bias Range
BEOL TDDB Rules
Enhanced Voltage Management

2

Expanding Richness of Design Collateral

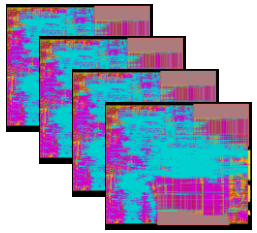
DDK Enhancements
RAM Compiler Enhancements
IO Enhancements

3

Enabling Auto Quality and Analog IP

Unique Design Rules & Verification
Supporting Multiple IP Vendors
Auto Aging Use Case

Single A53 @ >1.2 GHz



Lower Power & Smaller Area

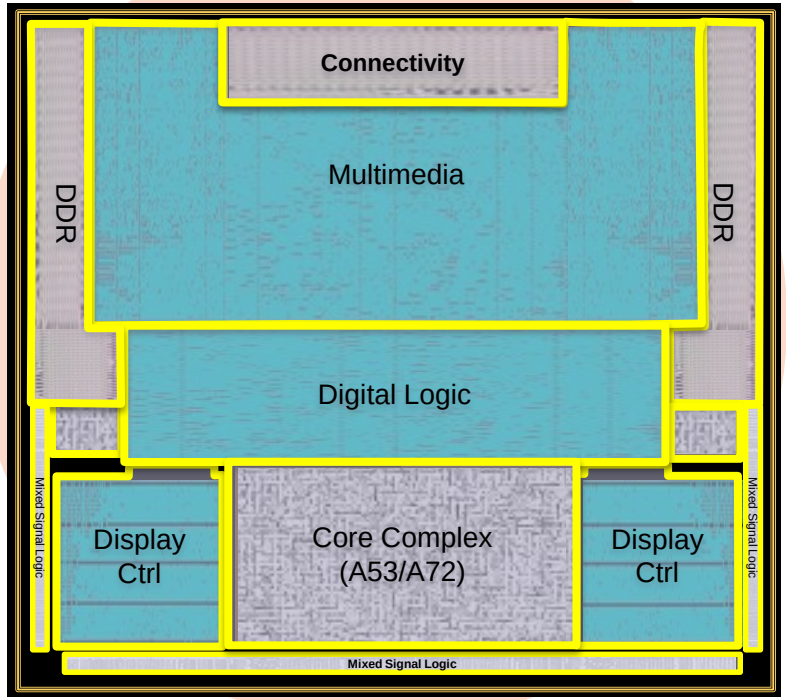
- Leveraging Bias Range
- Scalable Performance

Subsystem Attributes	28 FD SOI	Alternative 28nm
Leakage (Typical / WC)	70 / 175mA	125 / 315mA
Normalized dynamic power	0.75	1.0
Area	1.3 sqmm	1.7 sqmm

i.MX 8 Coming Soon…

Leveraging superset design…

- ARM® V8-A 64 bit architecture
- 10+ core complex
  - Cortex-A72, Cortex-A53
- Enhanced graphics
- Leadership 4k video
- Integrated vision
- Low power 4k multi-display
- Mixed signal
- Rich connectivity
- Compelling auto features



28nm Technology

Positioning FD SOI for leadership in broad market application processors

Summary

- The evolving smart world requires a broad range of application processors
- I/O counts, integrated PHYs and interface speeds are increasing
- Integration of functions in a cost effective technology is required for success
- 28 FD SOI offers advantages that allows scaling from small power efficient processors to high performance safety critical processors
- NXP’s broad i.MX product portfolio and technology adoption strategy enables cost-effective ground-breaking solutions
- Future roadmap for i.MX will leverage 14nm class devices in order to scale power-performance when market demand justifies higher cost and expense of development