Smart World – Secure, Connected, Low-Power, Scalable

**Internet of Things**
- Smart Hospitals
- Smart Homes
- Smart Cities
- Smart Energy
- Smart Highways

**Software**
- Ease-of-use
- Open-source
- Security
- Device Management
- Professional Services

**Solutions**
- Embedded Processing
- Connectivity Protocols
- Multi-Sensing Applications
- Video, Image, Graphics, Voice

**Technology Innovations**
- Advanced NVM, RF, Mixed Signal Analog, and Sensors integration
- Powerful, Secure, Low-Power
- MCUs & Application Processors
- System Miniaturization & Advanced Packaging

**Connected World**
- Connected Cars
- Connected Homes

**Smart World**
- Secure, Connected, Low-Power, Scalable
i.MX Driving Explosive Growth in Smart Vehicles & Smart Devices

Over 200M i.MX SOCs shipped to date

Over 35M vehicles enabled with i.MX since 2007

Leader in eReaders and Auto Infotainment MPU
i.MX 6 Series: Supreme Scalability and Flexibility
Leverage One Design into Diverse Product Portfolio

Scalable series of NINE ARM-based SoC Families

Expanded series for performance, power efficiency and lower BOM
Recently Announced i.MX 7D & 7S Advantages

**Advanced Heterogeneous Architecture**
- Single and Dual Cortex-A7
  - Core up to 1GHz
- Cortex-M4 up to 266MHz
- Offload Tasks
- Optimize Power
- Increase Security

**Unmatched Power Efficiency**
- 3x improvement in Power Efficiency vs i.MX 6
- 100 uW/MHz for Cortex-A7
- 70 uW/MHz for Cortex-M4
- One third the power consumed in the Low Power suspend mode (250uW) vs i.MX 6

**Enabling Flexible High Speed Connectivity**
- PCI-e v2.1
- Dual Gbit Ethernet with AVB
- DDR QuadSPI support
- eMMC 5.0

**Complete Security Infrastructure**
- Secure Boot
- Crypto H/W Acceleration
- Internal and External Tamper Detection
- Secure RAM
- DPA attack Resistance
- Secure JTAG
Processing Power Efficiency

Active Power (mW/MHz)

- ARM® Cortex®-M0+
- ARM Cortex-M4
- ARM Cortex-A9/Ax

Core Architecture Improvements

Core-only

90nm → 28nm

28nm for MPU & MCU
i.MX Processor Roadmap
Two New i.MX Platforms Based on 28nm FD SOI Technology

i.MX 6QuadPlus
i.MX 6Quad
i.MX 6DualPlus
i.MX 6Dual
i.MX 6DualLite
i.MX 6Solo
i.MX 6SoloX
i.MX 6SoloLite
i.MX 6UltraLite

ARM® v7-A

i.MX 8 series
Advanced Graphics & Performance
ARM® v8-A

i.MX 7 series
Power Efficiency
ARM® v7-A
Increasing Integration of Diverse Components

Diversification

<table>
<thead>
<tr>
<th>Precision Analog</th>
<th>RF</th>
<th>HV</th>
<th>NVM</th>
<th>Sensors</th>
<th>Biochips</th>
</tr>
</thead>
</table>

Miniaturization

180nm
130nm
90nm
65nm
40nm
28nm
14nm

Higher Value SoC & SiP Systems

Sense, Acquisition & Connectivity Functionality

Computational & Graphics Functionality

Leading-edge process nodes
(45, 32…14FF) driven mainly by digital SoC

Longer-lasting shrink nodes
(40, 28…??) offer mixed-signal integration opportunity
End Nodes of **TOMORROW**

Complete Integration

Scaled and all-in-one small, thin form factor package
Moore’s Law
“No Exponential is Forever…but Forever can be Delayed”
NXP Process Development Strategy

- **CMOS Platform-Based Technologies:**
  - Leverage foundry standard technology
  - Adapt for targeted applications

- **Differentiating Technologies:**
  - Focus on performance/features
  - High re-use >80% of the technology platform
  - Wholly-owned intellectual property
Smart Technology Choices

1. Which node?
2. Which process architecture?
28nm – ‘Last Simple Node?’

40nm to 28nm will be significant % of worldwide capacity in 2020
Cost Vs. Performance

i.MX Die Cost Comparison: 16FF vs 28FD

Die Cost 16FF/28FD

Relative Wafer Price
- 150%
- 175%
- 200%

Die Size

i.MX Processors
- Large range of die size
- Larger amount of analog
- Pads and overhead not scaling
- Future RF integration
NXP History Leveraging SOI

- NXP has developed 20+ processors over 3 generations of SOI technology
- Soft Error Rate (SER) is becoming an increasingly significant factor as SoC memory arrays continue to increase in size & density
- Bulk technology performs successively worse with each technology node
- SOI provides 5 ~ 10x better SER reliability and the gap is widening as geometries shrink
- 28 FD SOI benefits extend to 10-100X better immunity
<table>
<thead>
<tr>
<th>Technology</th>
<th>Intrinsic (Technology) SER</th>
<th>Product-Level SER</th>
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<tbody>
<tr>
<td>28nm Bulk Si</td>
<td>Moderate</td>
<td>Design techniques / protection</td>
</tr>
<tr>
<td>28nm FD-SOI</td>
<td>Low</td>
<td>Protection techniques depend on amount of memory and logic content</td>
</tr>
<tr>
<td>14/16nm FinFET</td>
<td>Low</td>
<td>Protection techniques depend on amount of memory and logic content</td>
</tr>
</tbody>
</table>
FD SOI Advantages

1. **Power-Performance Benefits**
   - Low Vdd with Performance
   - Improved Electrostatics
   - Scalable Platform

2. **Analog & RF Characteristics**
   - Better Gain, Matching, Noise
   - Gate 1st Integration

3. **Lower Risk Manufacturing**
   - Simple Integration / Fast TAT
   - Extends 28nm install base
   - Low complexity planar device
28nm FD-SOI Platform

Back-bias enables large dynamic operating range

Good power-performance at low voltages, temperatures (IOT standby mode)

Logic Gate Leakage/Performance Metric

T=25C
Vdd=0.8V, 1.1V

Each point represents simulated average over three X1 library cells from a unique Vt-L combination. Ignores interconnect impact, which is highly implementation dependent.
## Process Technology Implications

<table>
<thead>
<tr>
<th>28nm &amp; Beyond</th>
<th>High-K Metal Gate</th>
<th>FD-SOI</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Efficiency</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Cost Competitiveness</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Ease of Design</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Ease of Diversification</td>
<td>●</td>
<td>●</td>
<td>●</td>
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### Multi-Cores
- Power Management
- Performance
- Security / ARM® TrustZone

### Memory
- Secure Java / OS support
- Connectivity S/W stack

### Non-volatile Memory
- Program Complexity
- Data Collection

### RF Connectivity
- Wireless Everywhere
FD SOI Gaps Addressed by NXP

1. Utilizing Full Range of Back-Gate Biasing
   - Extended Bias Range
   - BEOL TDDB Rules
   - Enhanced Voltage Management

2. Expanding Richness of Design Collateral
   - DDK Enhancements
   - RAM Compiler Enhancements
   - IO Enhancements

3. Enabling Auto Quality and Analog IP
   - Unique Design Rules & Verification
   - Supporting Multiple IP Vendors
   - Auto Aging Use Case
# Single A53 @ >1.2 GHz

**Lower Power & Smaller Area**
- Leveraging Bias Range
- Scalable Performance

<table>
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<tr>
<th>Subsystem Attributes</th>
<th>28 FD SOI</th>
<th>Alternative 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage (Typical / WC)</td>
<td>70 / 175mA</td>
<td>125 / 315mA</td>
</tr>
<tr>
<td>Normalized dynamic power</td>
<td>0.75</td>
<td>1.0</td>
</tr>
<tr>
<td>Area</td>
<td>1.3 sqmm</td>
<td>1.7 sqmm</td>
</tr>
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</table>
i.MX 8 Coming Soon…

Leveraging superset design…

- ARM® V8-A 64 bit architecture
- 10+ core complex
  - Cortex-A72, Cortex-A53
- Enhanced graphics
- Leadership 4k video
- Integrated vision
- Low power 4k multi-display
- Mixed signal
- Rich connectivity
- Compelling auto features

28nm Technology

Positioning FD SOI for leadership in broad market application processors
Summary

- The evolving smart world requires a broad range of application processors
- I/O counts, integrated PHYs and interface speeds are increasing
- Integration of functions in a cost effective technology is required for success
- 28 FD SOI offers advantages that allows scaling from small power efficient processors to high performance safety critical processors
- NXP’s broad i.MX product portfolio and technology adoption strategy enables cost-effective ground-breaking solutions
- Future roadmap for i.MX will leverage 14nm class devices in order to scale power-performance when market demand justifies higher cost and expense of development