FD-SOI POWER OPTIMIZATION FLOW

Challenges to FD-SOI adoption

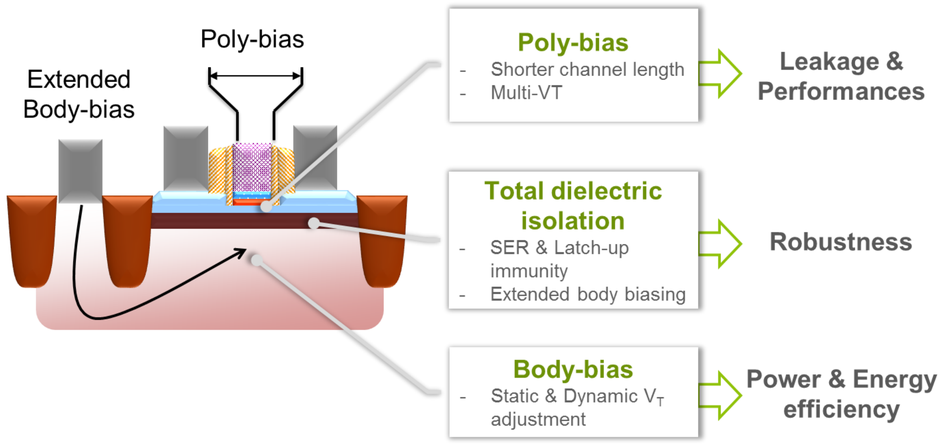
✓**Availability of multiple sources**
- There is now enough momentum with ST, Samsung and GlobalFoundries

✓**IP availability**
- Synopsys, Cadence, Invecas, and a number of smaller players are now providing (or will be) all the fundamental building blocks for SoC design in targeted markets

✓**Design porting in FD-SOI**
- The typical design flow for FD-SOI design is very similar to bulk
- Targeting a new design or porting an existing bulk design to FD-SOI requires little or no change in the existing design flows

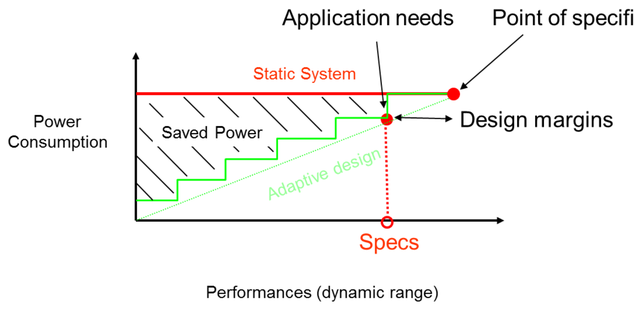
➢**Design optimization to minimize power consumption**
- However, a direct copy & paste approach will not provide the optimum result
- Early adopters, including Leti, have developed their own internal flows to leverage the unique features of FD-SOI to maximize device power and performance
- Need to streamline and automate these features to the benefit of the user community at large

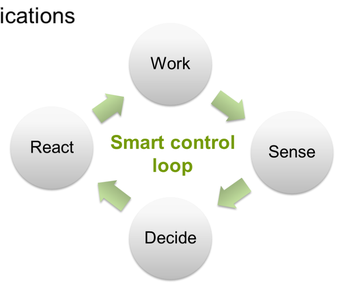
UTBB FD-SOI factors of merit

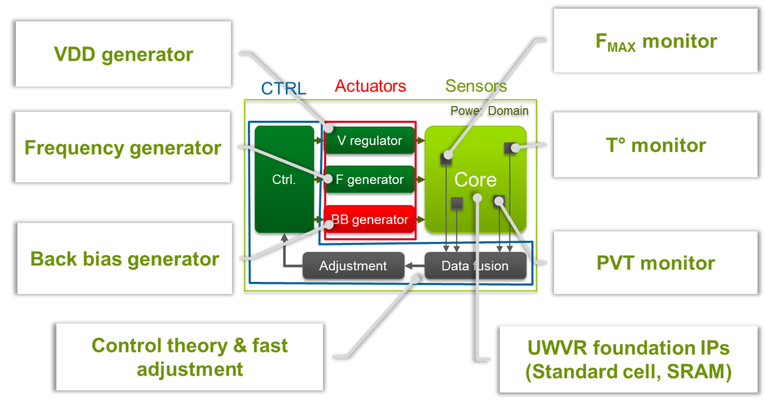


Fine granularity in power/performance optimization

Adaptative design



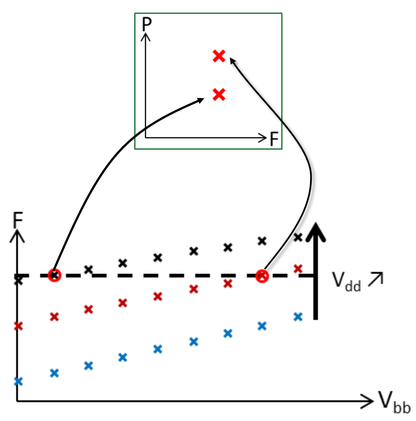


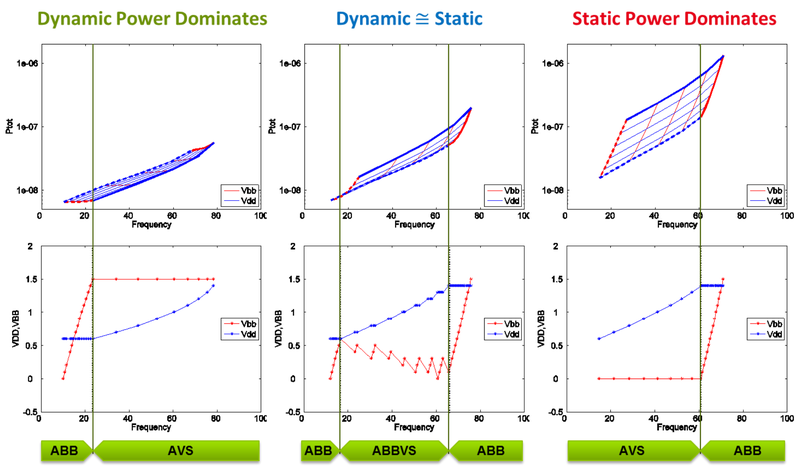


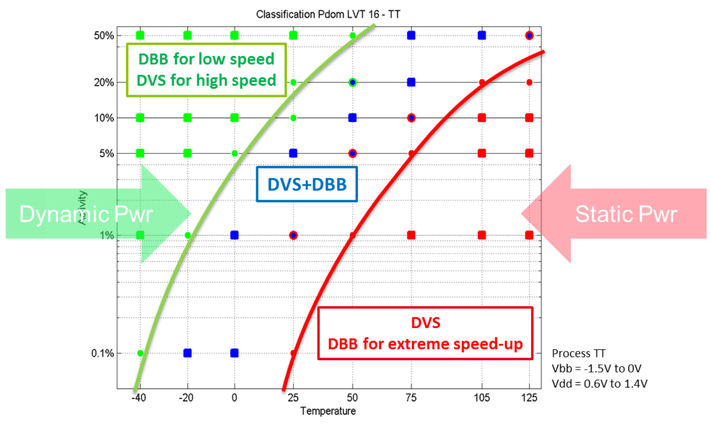
Towards Adaptive Voltage Frequency Scaling with ABB

Sense & React through smart control loop

Power management strategy: Balance between static and dynamic power

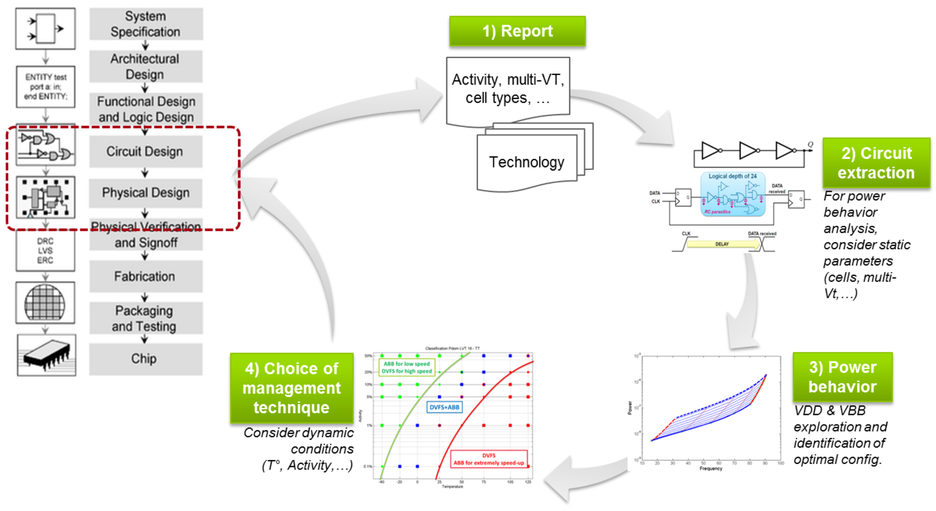


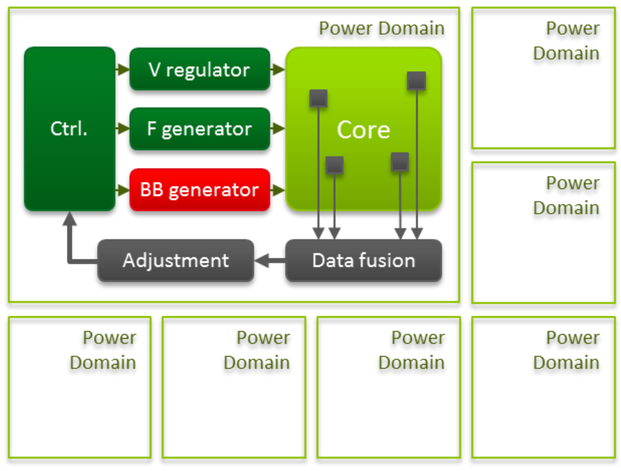




VDD and VBB chosen to minimize consumption

FD-SOI AVFS flow: A fine grain strategy per core





- ✓Sense & React IPs
- ✓Dynamic/Static optimization
- ✓Fine grain strategy per core
- ✓Automated optimization

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