Communication Infrastructure Disruptions Caused by the Forthcoming IoT Data Deluge: the \textbf{FD-SOI} Solution

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Digital and Mixed-Signal ASICs
A very interesting Time!
A time for radical Evolution, How to move forward?

**Semiconductor**
Moore’s law challenged
Opportunity for innovative solutions continuing Moore’s law
More than Moore: Integration, power, sensing, memories

**Digital Transformation**
In ALL activities
Connectivity revolutionizing progressively all businesses

**Pace of change Acceleration**
Opportunities and threats for all business sectors
New Applications / markets
Agility and innovation

Embrace change
Innovation
Agility
Disruption

Partner
Leverage Ecosystems
Identify Differentiating Partners

Do and Test Quickly - MVP
Small Steps
Incremental
Smart Things leverage the Internet
…and cause disruption

Modify existing Markets
Displace incumbents
Enable new entrants

Create new markets

Once a device or an activity becomes connected, it engages a (sometimes radical) transformation process
High Growth of Connected Objects

ANYTHING THAT BENEFITS FROM NETWORK CONNECTION WILL BE CONNECTED

Source: Intel

Source: Ericsson
Development of Pervasive Computing

All devices are **connected** and **share** their sensor state with the Internet to **optimize** computing.

**Drivers of growth**
- Increased network bandwidth
- Big data/analytics services
- Simple user interface
- Standards
- Security and privacy

**Requirements of semiconductors**
- Ultra-low power consumption: order of magnitude lower
- Cost: ultra-low cost

Source: GlobalFoundries
Connected Objects to generate a Data Deluge

- In 2010 (source IDC):
  - 1250 Billion Giga Bytes of data generated
    - more bits than stars in the universe
  - Already dominated by data coming from sensors
  - Storage (disk, ram, ...) capacity growing 30% slower than generated data

How much energy to transfer & process one?
Transporting data over the air (OTA): The Energy Dilemma (extreme case)

- Over the Air power efficiency:
  - Serial short reach link: best results around 0.5 pJ/bit
  - LTE: between 300 and 600 µJ/bit

Over The Air transportation power: 
\[ \Rightarrow \sim 30 \text{ to } 40 \text{ TWh} \]

World Electricity production growing at \sim 2\%/y 
\[ \Rightarrow \ 25.000 \text{ TWh in 2020} \]

Data Generated by Connected Objects expected to grow by \>1000 from ‘15 to ‘20

In 2020 Power from Wireless Transport part of Data Generated by Connected Objects would use over 100\% of the world Electricity production (including Heat, Car ...) !!!

OTA power efficiency to improve by \sim \times 10 \text{ max by 2020} (Silicon and RF technology improvements)

Data Generated by Connected objects have to be shrunk by several order of magnitude before OTA transmission

Data Quantity to Qualitative Data

*WW Elec in 2015 \sim 23.000 \text{TWh}
FUTURE: from IoT Data to IoT MetaData

Today

FUTURE

IoT Node

High Bandwidth → High Power

Limited Services because of large quantities of data to handle

IoT Node

Data

High Level / Value and more Services on MetaData

Structurally Enhanced Privacy / Security

Less Power and/or more supported IoT nodes
Semiconductor Technology
fuels market Innovation

Semiconductor process
Enable performance
Create requirements

Semiconductor Device
Enable performance
Create requirements

End Device
Enable performance
Create requirements

Applications
Create requirements
28nm FD-SOI
ST offering widest IoT Building Blocks

**Sensors & Actuators**
- Motion Sensors
- Environmental Sensors
- MEMS microphones
- Ranging & ambient light sensor
- FingerTip Touch Sensor
- MEMS mirrors

**Power Management**
- AMOLED power supply
- Backlight driver
- Power conversion
- Wireless charging
- Energy harvesting
- Thin film batteries

**ST Core Technologies**
- FD-SOI
- ULV
- RF
- Analog
  - MEMS
    - Time of Flight
  - SIP
    - Imaging
  - BiCMOS
    - eNVM
  - Silicon photonics
    - Smart Power

**Processing & Security**
- Low-power MCUs
- Secure MCUs
- Image analytics
- Sensor fusion
- EEPROM
- Dynamic NFC tags

**Connectivity, RF, Audio and Interfaces**
- ULP connectivity
- Positioning systems
- Mobile FEM
- Analog ICs
- Protection & EMI-filtering
- Audio processors & amplifiers
• ST **pioneered** FD-SOI technology & developed complete **Ecosystem**

• ST is now **Deploying** Products and ASIC services

• FD-SOI Key Factors of Merit
  • Power Efficiency
  • Analog / RF Design
  • Robustness
FD-SOI is unmatched for cost-sensitive markets requiring digital and Mixed Signal SoC integration and performance.

Factors of Merit:

- Power and energy efficiency
- Analog performance for mixed signal and RF design
- Robustness for mission critical applications

FD-SOI

FBB

0 $\rightarrow$ 1.3V

Total dielectric isolation
No channel doping
No pocket implant
**Energy Efficiency**

Test Chip Measurement on x4 Cores FD-SOI 28nm RVT

- **Max Freq. (MHz) → Perf. (OPS)**
  - 420MHz → 1.8GOPS
  - 2.4MHz → 10MOPS

- **Power at Max Freq. (mW)**
  - 0.2mW
  - 117mW

- **Energy Efficiency (MOPS/mW)**
  - Maximum at ~0.5V
  - Body Bias to manage dispersion

**Ultra Wide operating range**

Peak OPS/W competitive with best-in-class near threshold ULP µC and more than x100 peak OPS
Robustness Benefit

**Experimental Failure-in-Time (FIT) test data**

<table>
<thead>
<tr>
<th>ST 65nm Bulk</th>
<th>Vendor A 45nm Bulk</th>
<th>ST 45nm Bulk</th>
<th>Vendor A 28nm Bulk</th>
<th>ST 28nm Bulk</th>
<th>ST 28nm FD-SOI</th>
</tr>
</thead>
</table>

**SER Reduction w.r.t. BULK**

<table>
<thead>
<tr>
<th></th>
<th>FD-SOI</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alpha</td>
<td>1/1000×</td>
<td>1/15×</td>
</tr>
<tr>
<td>Neutron</td>
<td>1/100×</td>
<td>1/10×</td>
</tr>
<tr>
<td>Latchup</td>
<td>immune</td>
<td>not reported</td>
</tr>
</tbody>
</table>

- ECC not mandatory → Power and Area saving
- High Latch-up Immunity
- Larger Integrated Memory
- Rad-hard designs simpler

FD-SOI provides a more reliable platform for mission critical operation
28nm FD-SOI for AMS/RF
**Advantages in Analog Design**

**Efficient Short Devices**
- Efficient use of short devices:
  - High analogue gain @ Low L
  - Low Vt mismatch (Avt ~ 2mV·µm)
- Performance example:
  - A 1µm/100nm device has a DC gain of 80 & a CVt of only 6mV

**Improved Analog Perf.**
- Higher Gm for a given current density
- Lower gate capacitance
- Higher achievable bandwidth or lower power for a given bandwidth

**Improved Noise**
- Same normalized drain current noise between BULK and FD-SOI
- Lower noise variability for FD-SOI
- Improved noise in FD-SOI

*Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics*
Advantages in Analog Design-II

- **Flip-well devices:**
  - Large Forward Body Bias (FBB) range
  - Negligible control current

- Use back-gate as « VT tuning knob »:
  - Unprecedented ~250mV of tuning range for FD-SOI vs.
  - ~ 10’s mV in any bulk

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**Very large $V_T$ tuning range by FBB**

![Graph showing very large $V_T$ tuning range by FBB](image)

- ST 28nm LVT NMOS (typical)

- **FD-SOI (flip-well flavor/LVT devices)**

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**Courtesy, A. Cathelin, STMicroelectronics**
Analog Filter Design Example

- Filters with several 100's MHz bandwidth
  - PVT + ageing affect system operation
  - Need to tune/trim independently several parameters impacting overall system:
    - cut-off frequency,
    - linearity,
    - noise,
    - all for an optimal power consumption

Regular CMOS Tuning/trimming solution: Voltage regulator impacting directly the signal path behavior

FD-SOI revolutionary solution: individual transistors body biasing oxide-isolated from the signal path behavior
FD-SOI: Tuning gm with Vbody
OK: gm variation; OK: linearity

- New tuning knob (and off the signal path): VBBP and VBBN
- Compensate $V_{DD}$ variations
  - Tune gm back to nominal
  - Ensure constant linearity operation

Traditional compensation

Compensation with back-gate bias
Inverter-based Analog Filter

- RF low-pass Gm-C filter using CMOS inverters
  - Tuned by back-gate instead of supply (no signal path interference)
  - Supply regulator-free operation
    - Energy efficient
    - Low voltage operation (VDD = 0.7V)
  - Competitive linearity
- Compared to similar circuit in 65nm bulk [2], at same noise level, get X2 linearity for /4 power level
- Compared to best-in-class filters [7], at same noise level and Fc, get competitive linearity for /14 power level
- Best in class in terms of the compromise noise-linearity-power
- Integrated in ST 28nm FD-SOI CMOS

<table>
<thead>
<tr>
<th>Technology</th>
<th>This work</th>
<th>[2]</th>
<th>[5]</th>
<th>[6]</th>
<th>[7]</th>
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<tbody>
<tr>
<td>Technology</td>
<td>28nm FD-SOI CMOS</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>0.13um CMOS</td>
<td>0.18um CMOS</td>
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<tr>
<td>Order</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>3</td>
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<tr>
<td>Supply voltage [V]</td>
<td>0.7 0.8 0.9 1</td>
<td>1</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
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<tr>
<td>Cut-off freq. [MHz]</td>
<td>454 454 457 459</td>
<td>4700</td>
<td>275</td>
<td>200</td>
<td>300</td>
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<tr>
<td>Input ref. noise [nVrms/\sqrt{Hz}]</td>
<td>5.9 6.1 6.1 5.9</td>
<td>6.6</td>
<td>7.8</td>
<td>35.4</td>
<td>5</td>
</tr>
<tr>
<td>in-band IIP3 [dBVp]</td>
<td>1.2 4.0 4.0 2.4</td>
<td>-3</td>
<td>-12.5</td>
<td>4</td>
<td>6.9</td>
</tr>
<tr>
<td>Power diss. [mW]</td>
<td>4.0 4.6 5.2 5.6</td>
<td>19</td>
<td>36</td>
<td>21</td>
<td>72</td>
</tr>
<tr>
<td>SFDR/BW [dB/Hz]</td>
<td>109 110 110 109</td>
<td>105</td>
<td>98</td>
<td>100</td>
<td>113</td>
</tr>
<tr>
<td>SNR [dB]</td>
<td>137 139 138 137</td>
<td>125</td>
<td>111</td>
<td>117</td>
<td>131</td>
</tr>
</tbody>
</table>

[J. Lechevalier at al, ISSCC 2015]

**Advantages in RF/mmW Design**

### Active devices high frequency performance

- For ST 28nm FD-SOI LVNTFET: \( f_T \text{ / } f_{\text{max}} > 300\text{GHz} \)

- For RF operation frequency:
  - Work with \( L = 100\text{nm} \)
  - MAG = 12dB @ 10GHz
  - \( \text{NF}_{\text{min}} \sim 0.5\text{dB} @ 10\text{GHz} \)
  - Work @ current density: 125 \( \mu\text{A/\mu m} \)

- For mmW operation frequency (intrinsic models):
  - Work @ L_{\text{min}}
  - MAG = 12dB @ 60GHz
  - \( \text{NF}_{\text{min}} \sim 1.3\text{dB} @ 60\text{GHz} \)
  - Work @ current density: 200 \( \mu\text{A/\mu m} \), 33% less power than in 28LP bulk

### Performant passive devices

- Operation frequency range: 2 GHz - 50 GHz
- Inductance range: 0.1 nH - 28 nH
- Q factor range: 20 - 35
- Size: 60x60 \( \mu\text{m}^2 \) – 600x600 \( \mu\text{m}^2 \)

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*Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, C. Durand STMicroelectronics*
**60GHz Configurable PA**

- Fully WiGiG compliant (linearity and frequency range)
- New PA architecture: continuously reconfigurable power cells
- Continuous operation class tuning thanks to body bias with 2 extreme modes:
  - High gain mode: Highest ITRS FOM
  - **10X better than previous SoA**
  - High linearity mode: Break the linearity / consumption tradeoff
- ULV high efficiency operation (Vdd\_min = 0.8V)
- Integrated in ST 28nm FD-SOI CMOS

<table>
<thead>
<tr>
<th>This work</th>
<th>S. Kulkarni *ISSCC2014*</th>
<th>D. Zhao *JSSC2013*</th>
<th>D. Zhao *JSSC2012*</th>
<th>E. Kaymaksut *RFIC2014*</th>
<th>A. Siligaris *JSSC2010*</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>28nm UTBB FD-SOI</td>
<td>40nm</td>
<td>40nm</td>
<td>40nm</td>
<td>40nm</td>
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<tr>
<td>Operating mode</td>
<td>High gain</td>
<td>High linearity</td>
<td>NA</td>
<td>Low/High power</td>
<td>NA</td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>1.0</td>
<td>1.0</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
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<tr>
<td>Freq. [GHz]</td>
<td>61</td>
<td>60</td>
<td>60</td>
<td>63</td>
<td>61</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>35</td>
<td>15.4</td>
<td>15.1</td>
<td>22.4</td>
<td>16.8 / 17</td>
</tr>
<tr>
<td>P_SAT [dBm]</td>
<td>18.9</td>
<td>18.8</td>
<td>16.9</td>
<td>16.4</td>
<td>12.1 / 17</td>
</tr>
<tr>
<td>P_1dB [dBm]</td>
<td>15</td>
<td>18.2</td>
<td>16.2</td>
<td>13.9</td>
<td>9.1 / 13.8</td>
</tr>
<tr>
<td>PA_max [%]</td>
<td>17.7</td>
<td>21</td>
<td>21</td>
<td>23</td>
<td>22.2 / 30.3</td>
</tr>
<tr>
<td>PA_1dB [%]</td>
<td>9</td>
<td>21</td>
<td>21</td>
<td>18.9</td>
<td>14.1 / 21.6</td>
</tr>
<tr>
<td>PAE_8dB_backoff [%]</td>
<td>1.5</td>
<td>8</td>
<td>7.5</td>
<td>3</td>
<td>- / 4.7</td>
</tr>
<tr>
<td>P_DC [mW]</td>
<td>331</td>
<td>74</td>
<td>58</td>
<td>88</td>
<td>56 / 75*</td>
</tr>
<tr>
<td>P_DC_8dB_backoff [mW]</td>
<td>332</td>
<td>124</td>
<td>84</td>
<td>94</td>
<td>56 / 78*</td>
</tr>
<tr>
<td>100*P_1dB/P_DC</td>
<td>9.6</td>
<td>89</td>
<td>72</td>
<td>28</td>
<td>14.5 / 32*</td>
</tr>
<tr>
<td>Active area [mm²]</td>
<td>0.162</td>
<td>0.081</td>
<td>0.074</td>
<td>0.33</td>
<td>0.1</td>
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<tr>
<td>ITRS FOM [W.GHz²]</td>
<td>161,671</td>
<td>1,988</td>
<td>1,198</td>
<td>6,925</td>
<td>641 / 2,832</td>
</tr>
</tbody>
</table>

*ITRS FOM = P\_SAT.PAE\_max.Gain.Freq²*  
\*: with pads  
\#: estimated

[A. Larie et al., ISSCC2015]
Takeaways

- Smart connected applications (IoT) will cause major market **Disruptions**
  - Innovate, **Partner**, Do, Test

**Disruptive Silicon** technologies & IPs
- FD-SOI brings Energy Efficiency Digital and AMS Breakthrough for IoT

**FD-SOI** for AMS/RF design
- For Analog/RF design:
  - FBB as VT tuning knob ➔ ultra large tuning range for VT
  - Very good analog performance ➔ lower power consumption and operate at L>Lmin for design margin
- For RF/mmW design, operate at Lmin and add deep subµ technology features
  - Front-end: performant $f_T$, $f_{max}$
  - Back-end + FD-SOI features: performant passive devices
Thank you!