Realize the Potential of FDSOI in Growing Markets

ARM

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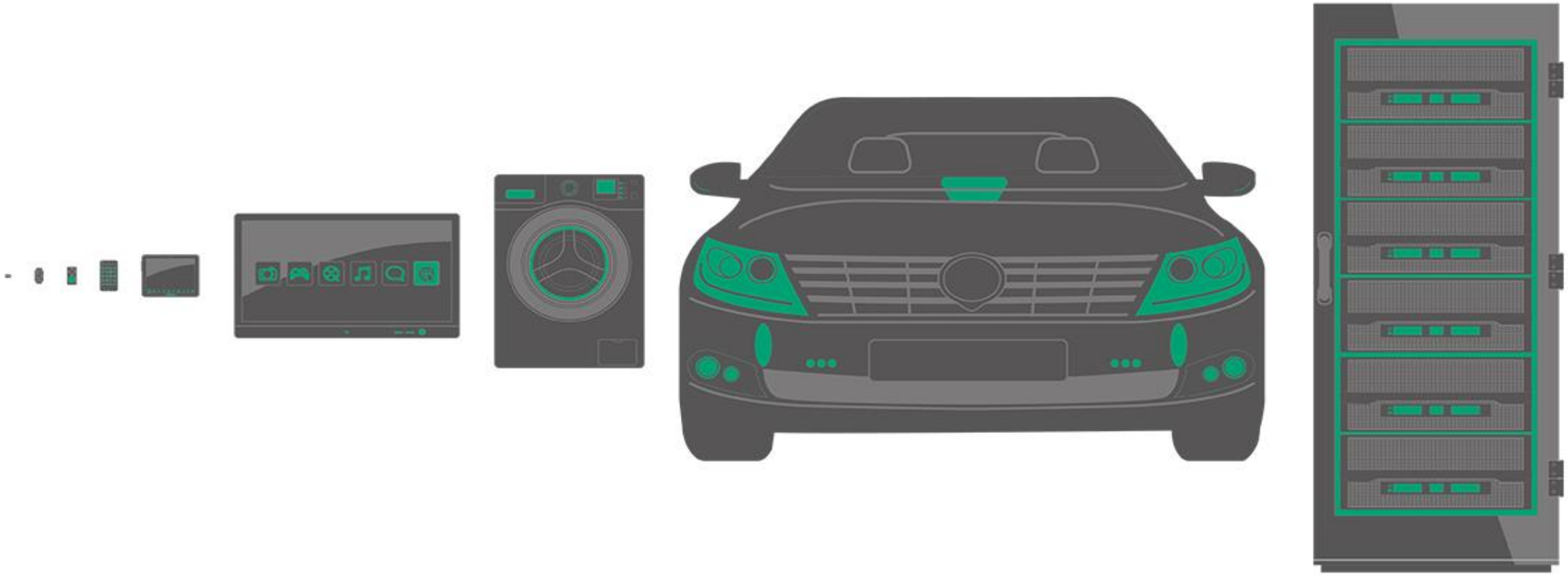
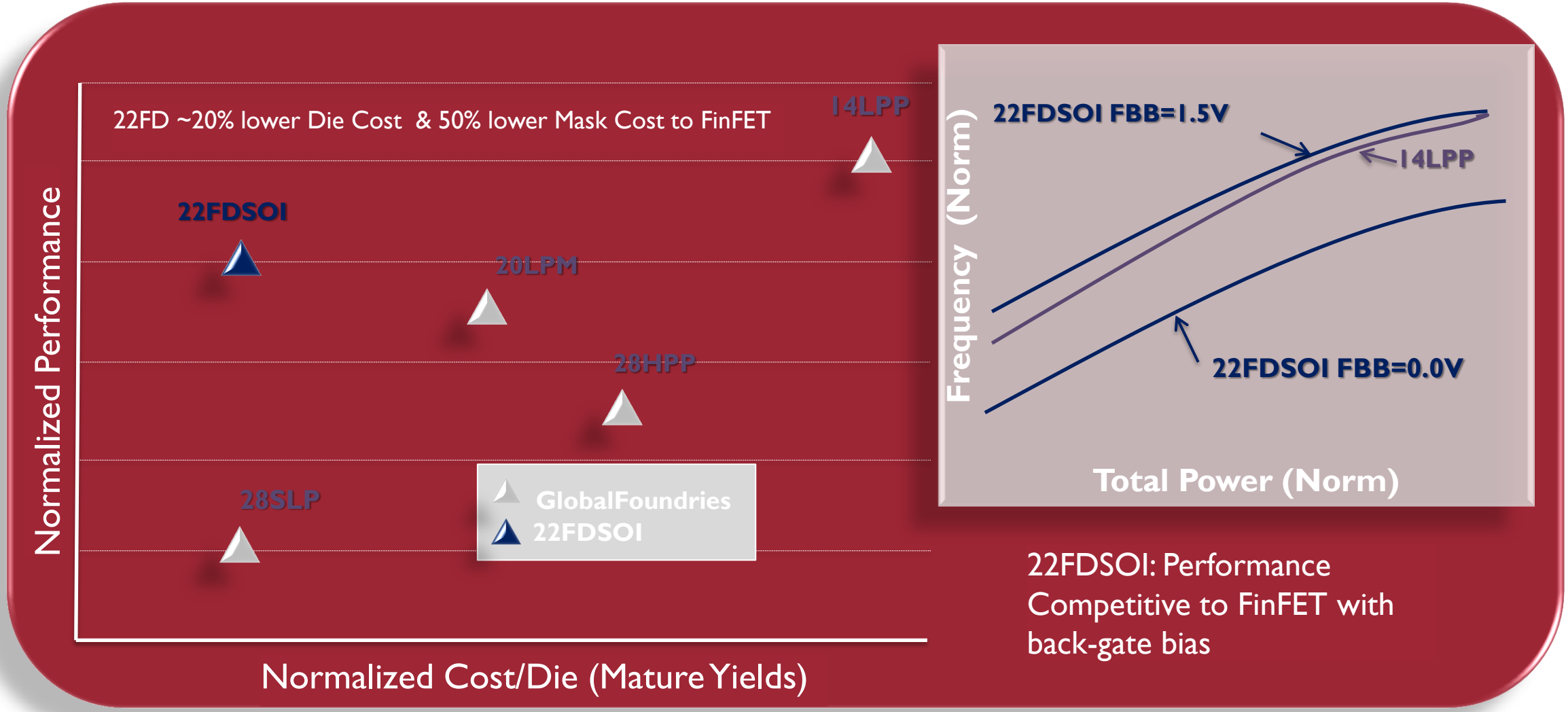
Market Trends Shaping the Semiconductor Industry



Planar Fully Depleted SOI 22FDSOI Technology Analysis

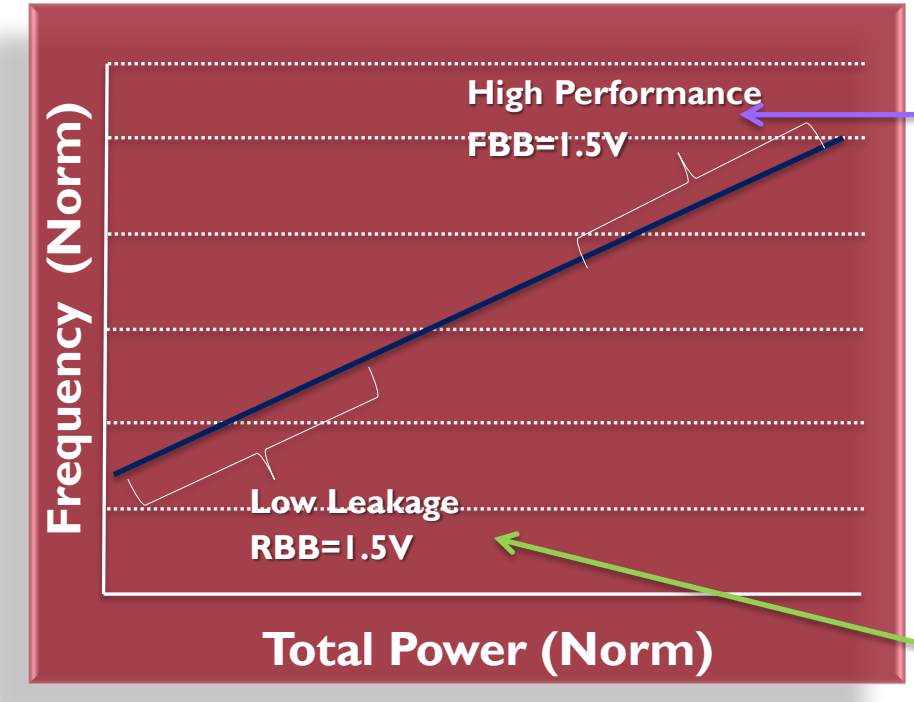
22FDSOI Technology Cost-effective Alternative to FinFETs?



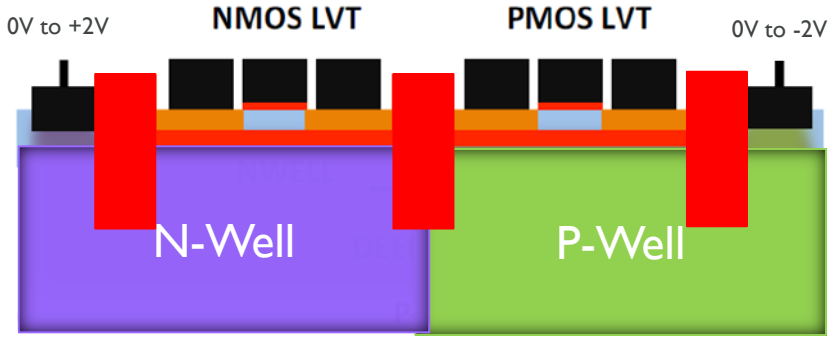
22FDSOI: Performance Competitive to FinFET with back-gate bias

Power/Performance Flexibility with Dynamic Back-Gate Bias

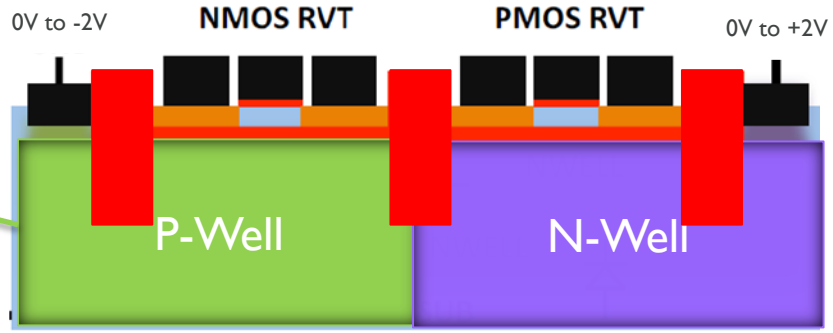
- Transistors architected for Back-Gate Biasing (BB)
- High-performance operation with Forward BB (FBB)
- Ultra-low voltage operation with Forward BB (FBB)
- Ultra-low leakage with Reverse BB (RBB)



High Performance Flip Well Transistor

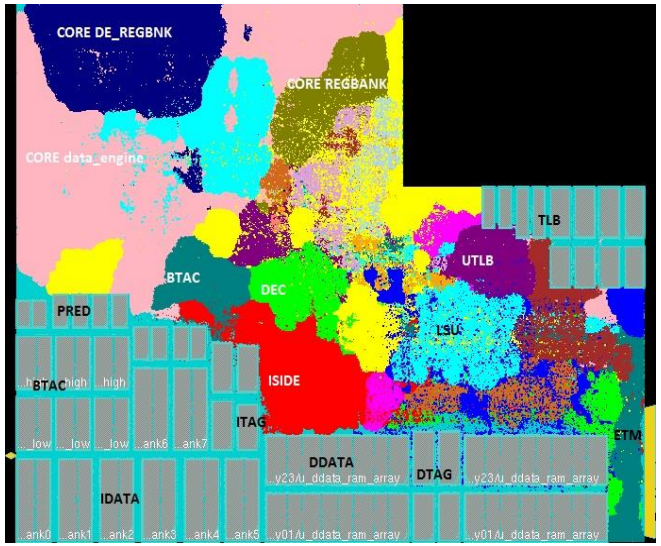


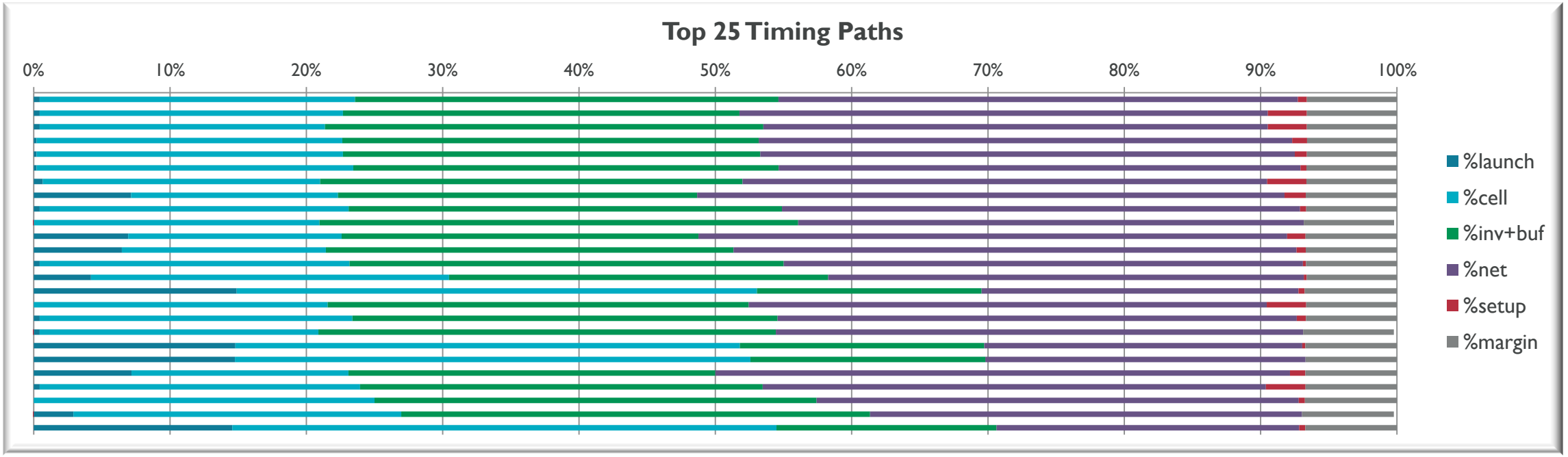
Low Leakage Conventional Well Transistor



ARM POP™ IP Benchmark Reference

- 14LPP optimized high-performance POP IP – 2.6GHz (TT/0.9V/85c)
  - Detailed analysis of Timing Paths
- ARM Artisan® Physical IP Figure of Merit (FOM)
  - Measures tradeoffs of logic & memory architectures
  - Transistor and wire contribution
- Combine FOM with Timing Path Data for accurate new technology predictions





Total Path Delay = %launch + %cell + %inv+buf + %net + %setup + %margin

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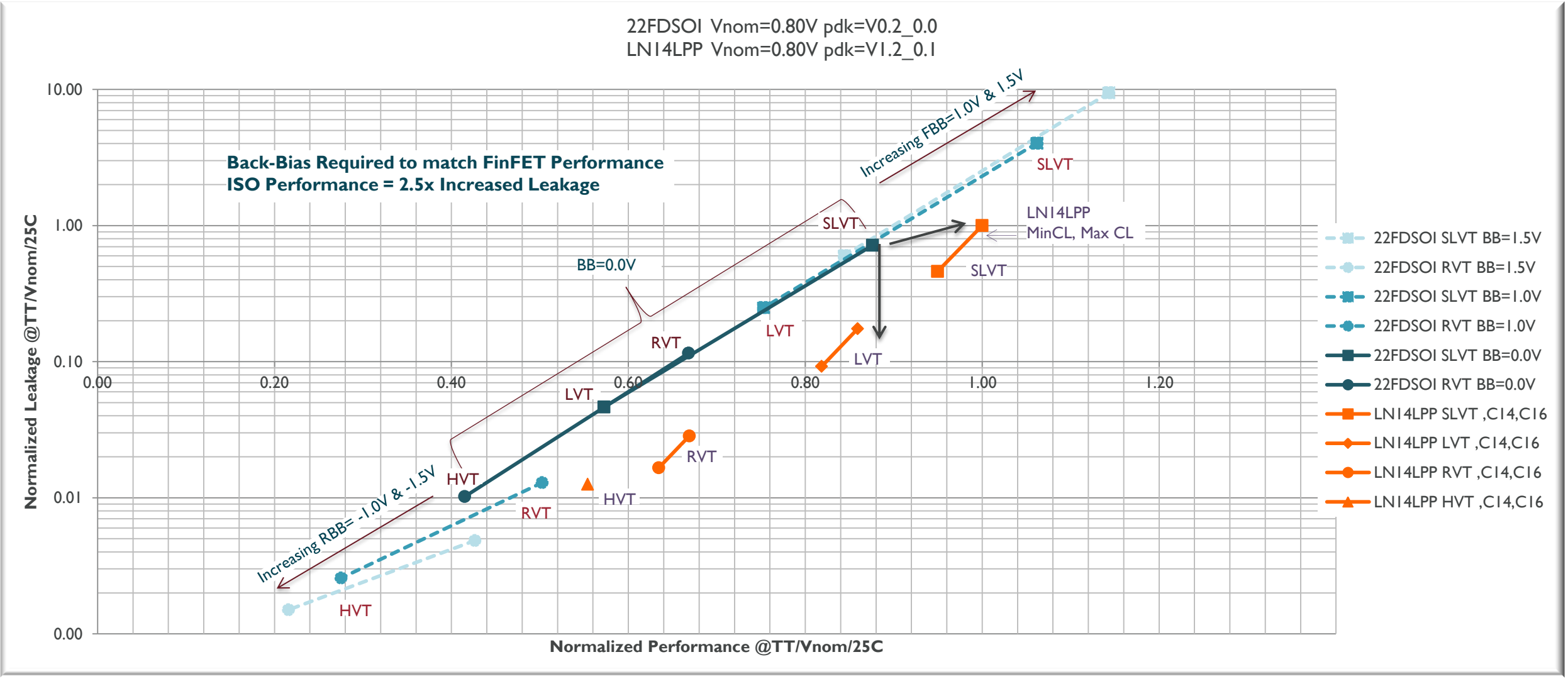
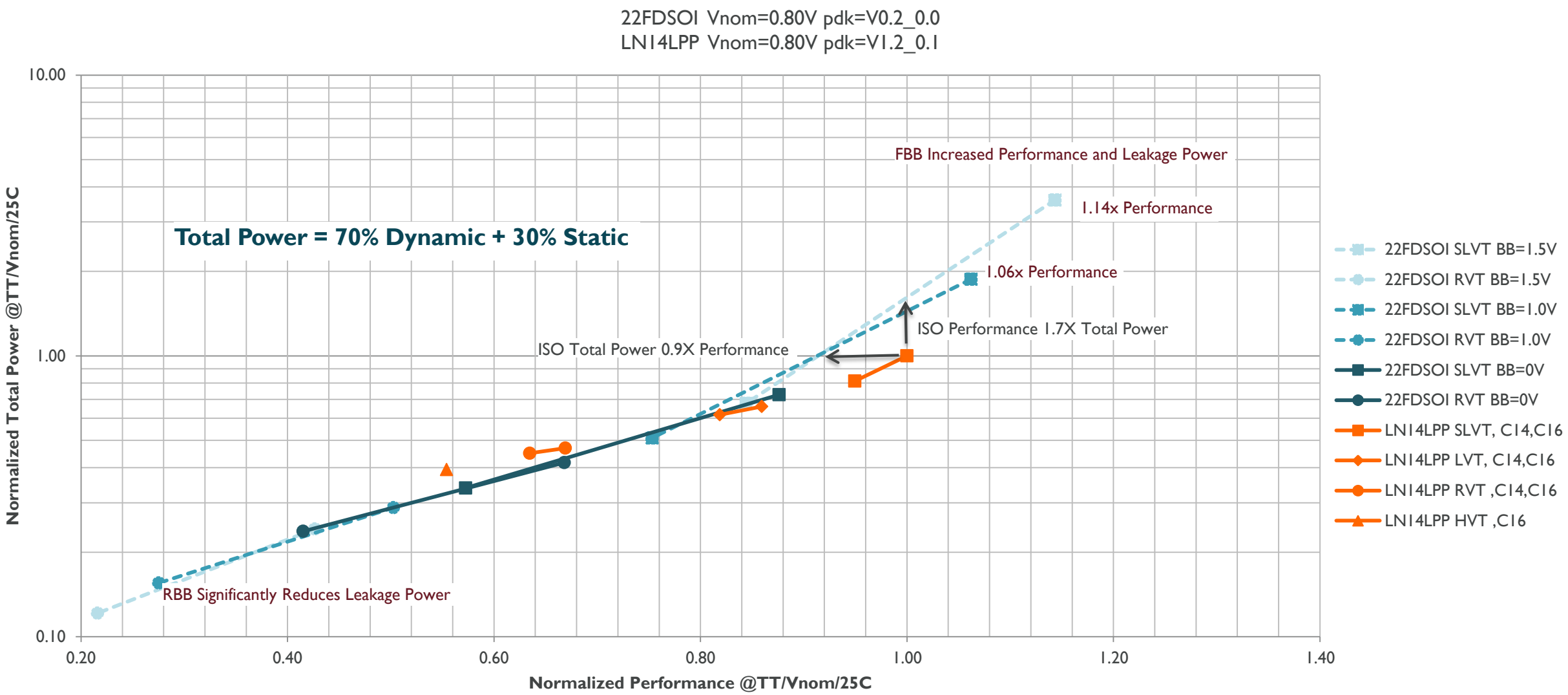
Leakage vs. Performance FOM Evaluation



22FDSOI Measurements are made on early PDK (V0.2_0.0) release and early wire length estimations and may adjust with future Process Releases

Total Power (Single Implant) vs. Performance



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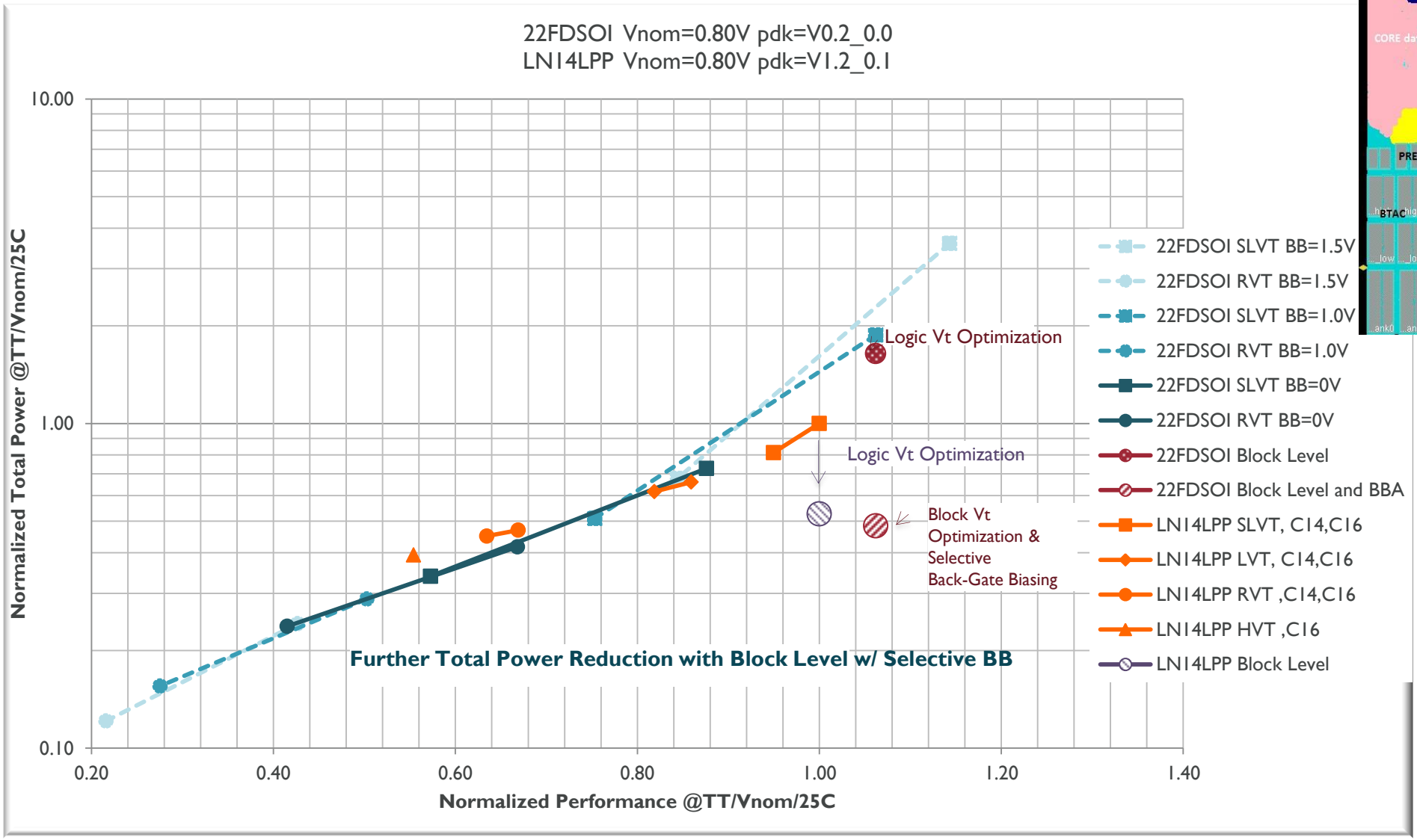
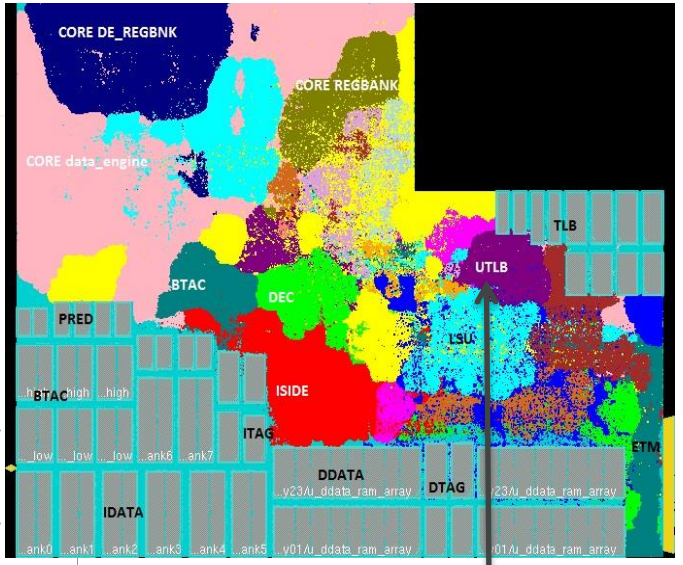
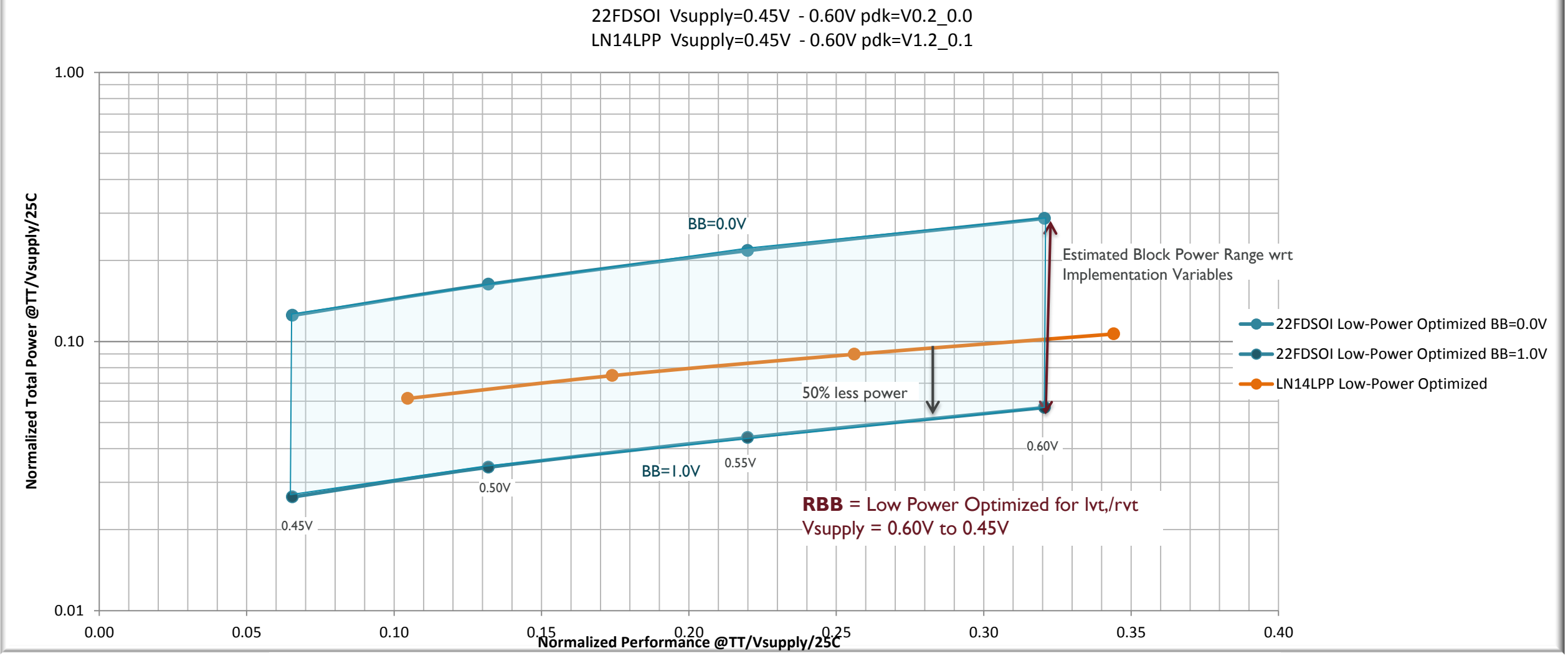
Total Power vs. Performance





Selective Back-Gate Biasing concept is in early research and development, final total block power reduction with BBA is an early projection.

Total Block Level Power vs. Performance @Various Vsupply



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22FDSOI FOM Benchmark Summary

- Optimized with POP IP and using proper back-gate bias on FDSOI, ARM high-performance CPUs such as ARM Cortex®-A72 can achieve similar performance to FinFET technology
  - Back-gate bias can be adjusted dynamically so it allows "performance-on-demand" and power efficiency when the performance is not needed.
- With proper reverse back-gate bias, extremely power-efficient applications such as IoT that uses Cortex-A32/A35 cores on FDSOI can achieve superior total power
- To take advantage of the full FDSOI back-gate optimization opportunities such as selective block level biasing, knowledge in ARM microarchitecture implementation is required
- Detailed implementation knowledge, or the use of ARM CPU POP IP provides insight to maximize the technology entitlement from new technology such as FDSOI

Selective Back-Gate Biasing concept is in early research and development.

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Thank You