Enabling Next Generation Semiconductor Product Innovations with 22FDX™

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Vice President, CMOS Platforms Business Unit
GLOBALFOUNDRIES - Company Highlights

**Revenue**

- ~6B* $

**More Than**

- 25,000 Patents & Applications
- 250 Customers
- ~18,000 Employees

Global Manufacturing Capacity: ~7M Wafers/Yr**

- **TECHNOLOGY**
  - 90nm–22nm
  - 28nm, ≤ 14nm
  - 350nm–90nm
  - 45nm–28nm
  - 180nm–40nm

- **CAPACITY IN WAFERS/MONTH**
  - East Fishkill, New York: 14,000 (300mm)
  - Malta, New York: Up to 60,000 (300mm)
  - Burlington, Vermont: 40,000 (200mm)
  - Dresden, Germany: 60,000 (300mm)
  - Singapore: 68,000 (300mm)
  - 93,000 (200mm)

*Based upon analysts’ estimates

**200mm Equivalents
Estimated IoT Semiconductor Value 2019–2020 ($50B–$75B)

Semiconductor device market value of "Smart Things" in the Internet of Things\(^1\)

- Wearables: $4–5B
- Consumer Electronics: $7–11B
- Smart Home: $12–15B
- Smart Buildings: $10–15B
- Smart Cities: $5–10B
- Industrial Automation: $3–4B
- Medical: $7–10B
- Nascent Verticals: $2–4B

Barriers:
- Standardization
- Fragmentation
- End-to-end solutions
- Business Models
- Security
- Low power

Cost and Energy Efficiency will be Key Drivers of Product Innovations

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\(^1\)Excluding is "classic internet devices" such as laptops, smartphones. Also excludes automotive applications. Rough preliminary estimate with indicative split by device type. Integration of simple devices with communication features and memory in SoCs assumed and accounted for in communications category, embedded memory under logic.

Source: McKinsey & Company, based on volume forecast by Gartner, iSupply, Strategy Analytics
**COST:** The economic foundation on which the semiconductor industry has functioned for 4 decades – is at risk…

Wafer cost increase driven by scaling and compounded by FINFET and double patterning requirements

Node Migration economics is changing.

**Net result:**
The era in which shrinking features automatically ensured >30% cheaper transistors is over!
Energy Efficiency: 0.4V is the Minimum Energy Point for almost any Technology

Most optimum energy operating point is around 0.4V
- As Vdd decreases dynamic power goes down drastically while frequency also goes down
- Leakage power also goes down as Vdd drops
- Energy goes up below ~0.4V Vdd since delay increases result in crow-bar current increase, overshadowing dynamic power reduction
Industry Research: FDSOI SRAM remains functional down to VDD=0.4V

FDSOI 0.08um2 SRAM (80nm CPP)

- SRAM Stability and Vt Variability Improvement with Back Bias
- Clear SNM modulation from back bias
- Both Stability and Vt variation improved with Back-bias
Introducing 22FDX™ Platform

- **Industry’s first 22nm** fully-depleted silicon-on-insulator technology
- Ultra-lower power with **0.4 volt operation**
- **Software-controlled transistor body-biasing** for Innovative performance and power optimization
- Delivers **FinFET-like performance** and better energy-efficiency at 28nm-like cost
- Integrated RF: reduced system cost, and back-gate feature to **reduce RF power up to ~50%**
- **Post-Silicon Tuning/Trimming** for Analog/RF, SRAM and Power/Performance optimization
- Enables Innovative applications across **Mobile, IoT and RF markets**
22FDX™ offers the widest range of Performance/Leakage Optimization points

**Relative Performance**
- 1.0
- 0.8
- 0.6
- 0.4
- 0.2
- 1.2

**Relative Leakage**
- 1
- 10
- 100
- 1000
- 10000
- 100000
- 1000000

**SLVT/LVT**
- Lowest $V_T$
- Optimized for FBB
- Highest performance

**RVT/HVT**
- Mid-range $V_T$
- Optimized for RBB
- Balance of low leakage and high performance

**ULL**
- Optimized for leakage
- Coupled with RBB achieves $\approx 1$ pA/um leakage

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22FDX™ Solutions for IoT/Wearables

Energy Efficient
- Ultra-low power to 0.4v
- Ultra-low leakage to 1pA/um
- Software controlled body bias
- >80% power savings

Superior Connectivity
- Superior RF/Analog devices
- RF IP for Wi-Fi/BLE
- Integrated RF for lower BOM

Cost Effective
- 50% less area than 28HKMG in A7 core
- 35% fewer masks than FinFet

\[ P_{\text{avg}} = P_{\text{always-on}} + \frac{E_{\text{active}}}{T_{\text{wkup}}} \]
ARM Cortex A7 Implementation – Initial results

22FDX is the First Technology to demonstrate 0.4V operation capability at >500Mhz on an ARM A7 Processor

- FinFet like Performance (1.2Ghz)
- 50% faster performance and 18% lower power than 28HKMG
- 47% lower power than 28HKMG at Iso-Frequency
- 92% Less Power at 520MHz (wrt 28HKMG at 800MHz)

Source: Verisilicon
Next Generation SoC Products leverage 22FDX™
RF Value

Low-power, High-performance RF and precision analog

<table>
<thead>
<tr>
<th>RF Feature</th>
<th>Analog/RF benefit</th>
</tr>
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<tbody>
<tr>
<td>High transconductance-to-drain current ratio (Gm/I)</td>
<td>= Low power &amp; high performance of RF circuits</td>
</tr>
<tr>
<td></td>
<td>• &gt;40% power reduction for LO chain, IQ gen, RF dividers</td>
</tr>
<tr>
<td></td>
<td>• &gt;25% power reduction for PA driver and integrated PA</td>
</tr>
<tr>
<td>Superior transistor matching of 1.5mV-um</td>
<td>= Improved matching performance or lower area for better matching. Smaller area = Lower power.</td>
</tr>
<tr>
<td>Threshold voltage modulation through back-gate</td>
<td>= Performance and power for LO generation circuits</td>
</tr>
<tr>
<td>More flexible layout configurations than FinFET</td>
<td>= Easier analog design migration from mature nodes</td>
</tr>
<tr>
<td>High fT and fMax</td>
<td>= Enables low-power 5G and mmWave products</td>
</tr>
<tr>
<td>Back-gate for circuit calibration, trimming and tuning</td>
<td>= Mitigates process variations and allows “off-signal path” calibration schemes</td>
</tr>
<tr>
<td></td>
<td>• Fix clock or LO signal skews w/o interfering with signal path</td>
</tr>
<tr>
<td></td>
<td>• Improves time-to-market by eliminating RF design respins</td>
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GLOBALFOUNDRIES Proprietary
22FDX™ enables System level Integration without the need for multiple heterogeneous technologies.

Cost Per Function and Energy Efficiency are the two most important metrics for next wave of Innovations.
ARM Cortex-A17 Quad-core Implementation using Industry Standard EDA tools (ARM TechCon 2015):

- Successful Cortex-A17 quad-core implementation using:
  - 5 power domains (4 CPU cores + 1 nonCPU module)
  - 5 body-bias net pairs (n-well, p-well biasing)
    - 1 pair for standard cells
    - 2 pairs for L1 cache periphery, bitcell array
    - 2 pairs for L2 cache periphery, bitcell array
    - Body-bias nets might be shared depending on eventual IP features

- Used our reference flow capability

- Coming Soon:
  - Hierarchical low power flow (VDD and BB scaling control)
  - In-design added modules (DRC/PM/MetalFill)
  - Power and signal EMIR modules
  - Integrate BB IP to generate the bias voltages
Easy Design Migration from Bulk node to 22FDX™

**BEST PAPER AWARD FOR 22FDX™ @SNUG 2016**

**Design Planning (FBB vs RBB)**
- Library Char + POCV/LVF variability
  - Lib char with BB (Added corners)

**RTL Synthesis**
- UPF Connectivity
  - Cell placement + Tapcell Placement + CTS pre-route
  - Implant-aware

**Routing Optimization**
- Tapcell connections (BB mesh + HV rules)

**Physical Verification + EMIR**
- Sign-Off PEX/STA (+DPT extraction)
  - Optional: Add sign-off Corners for dynamic BB variables (PVTB)

**In-Design Modules (DRC + PM + MetalFill + EMIR)**
- Optional: use FBB/RBB performance/power optimization

**Routing Optimization**
- Leakage recovery with VT swapping + Lgate optimization

**Legend**
- Same Step as Bulk
- New Step for 22FDX

Starter kit of 22FDX digital design flow available Today

Nov 2015: Ansys, Atoptech, Cadence, Mentor, Synopsys announced EDA support for 22FDX™
<table>
<thead>
<tr>
<th>IP Type</th>
<th>IP Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foundation IP</td>
<td></td>
</tr>
<tr>
<td>Standard Cells</td>
<td>High Density, High Performance</td>
</tr>
<tr>
<td>Memory Compilers</td>
<td>(a)High Density Single-Port SRAM</td>
</tr>
<tr>
<td></td>
<td>(b)High Speed Single-Port SRAM</td>
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<tr>
<td></td>
<td>(c)High Density Single-Port Register File</td>
</tr>
<tr>
<td></td>
<td>(d)High Speed Single-Port Register File</td>
</tr>
<tr>
<td></td>
<td>(e)High Speed Two-Port Register File</td>
</tr>
<tr>
<td></td>
<td>(f)High Density Via ROM</td>
</tr>
<tr>
<td>GPIO</td>
<td>Voltagess TBD and interfaces (SPI, I2C, MMC)</td>
</tr>
<tr>
<td>eFuse</td>
<td>4K macro</td>
</tr>
<tr>
<td>PLL</td>
<td>2-3 PLLs; Frequency, Jitter, Area, Power TBD</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>Support for multiple remote monitors</td>
</tr>
<tr>
<td>OTP</td>
<td>One-Time Programmable</td>
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</table>
## Full range of Complex IP – Under Development

<table>
<thead>
<tr>
<th>IP Type</th>
<th>IP Description</th>
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</thead>
<tbody>
<tr>
<td>Complex IP</td>
<td>PCIe 1.1 (x1); XAUI 3.125</td>
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<tr>
<td></td>
<td>PCIe 2.0 (x1, x4); XAUI 6.125</td>
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<tr>
<td></td>
<td>PCIe3 (Root and endpoint 2.5/5.0/8.0Gb/s)</td>
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<td></td>
<td>USB3.1 (5/10Gb/s)</td>
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<td></td>
<td>SATA (Gen 1, 2, and 3)</td>
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<tr>
<td></td>
<td>Ethernet 1 – 10G BP KR</td>
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<tr>
<td>1-12.5G Multi-protocol SERDES</td>
<td>USB2 PHY</td>
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<tr>
<td></td>
<td>USB2.0 HOST and OTG</td>
</tr>
<tr>
<td>DDR3/DDR4</td>
<td>DDR3 up to 2400, DDR4 up to 3600</td>
</tr>
<tr>
<td>LPDDR3/LPDDR4</td>
<td>LPDDR3 2133, LPDDR4 4267</td>
</tr>
<tr>
<td>DPHY</td>
<td>MIPI DPHY (CSI2, DSI) [4lanes; 12 Bit]</td>
</tr>
<tr>
<td>MPHY or CPHY</td>
<td>MIPI MPHY (SSIC/UFS2) with Gear3 support</td>
</tr>
<tr>
<td>DP/HDMI/MHL 2.x – TX</td>
<td>Combo, HDMI2.x (6Gb/s), DisplayPort1.3 (8.1Gb/s)</td>
</tr>
<tr>
<td>DP/HDMI/MHL 2.x – RX</td>
<td>DisplayPort (5.4Gb/s), HDMI2.x (6Gb/s)</td>
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<tr>
<td>Frac PLL</td>
<td>1 GHz, Low Jitter PLL</td>
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<tr>
<td>Video DAC</td>
<td>24b Audio DAC</td>
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<tr>
<td></td>
<td>2-Channel</td>
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<tr>
<td>16b SAR Audio ADC</td>
<td>16b SAR Audio ADC</td>
</tr>
<tr>
<td>Body Bias Generator</td>
<td>2 Channel</td>
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<tr>
<td>RF IP</td>
<td>Body Bias Generator</td>
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<tr>
<td></td>
<td>Modular Design</td>
</tr>
<tr>
<td>RF IP</td>
<td>WiFi (802.11AC), 802.15.4, Blue Tooth LE</td>
</tr>
</tbody>
</table>
## FDSOI – The Road Ahead

### 22FDX™ Differentiated features will be extended to 10nm and beyond

<table>
<thead>
<tr>
<th>FDSOI Scaling</th>
<th>FinFET Scaling</th>
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</thead>
<tbody>
<tr>
<td>Strong industry support today – Ecosystem being established on an accelerated pace</td>
<td>Ecosystem established</td>
</tr>
<tr>
<td><strong>Scaling roadmap</strong></td>
<td><strong>Scaling roadmap</strong></td>
</tr>
<tr>
<td>- Power/Perf demonstrated w/ 14FD</td>
<td>- Good electrostatic demonstrated</td>
</tr>
<tr>
<td>- Boosters defined down to 10FD</td>
<td>- Higher effective Device width</td>
</tr>
<tr>
<td>- SRAM scaling demonstrated to 7nm</td>
<td>- Industry exploring Nano-wires at 7nm</td>
</tr>
<tr>
<td><strong>Lower Cost / Die</strong></td>
<td><strong>Higher Cost &amp; Higher complexity</strong></td>
</tr>
<tr>
<td>- Fewer mask layers</td>
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<tr>
<td>- Faster learning cycles</td>
<td></td>
</tr>
<tr>
<td><strong>Back-Gate bias (Software controlled)</strong></td>
<td><strong>Back Bias not as Effective</strong></td>
</tr>
<tr>
<td>- Process / Variability compensation</td>
<td></td>
</tr>
<tr>
<td>- Flexible Dynamic vs. Static Power</td>
<td></td>
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<tr>
<td><strong>Low-Leakage Devices &amp; Memory</strong></td>
<td><strong>Higher Leakage in a given foot-print (3D)</strong></td>
</tr>
<tr>
<td>- Reverse body-bias enhances further</td>
<td></td>
</tr>
<tr>
<td><strong>Lowest Vmin Device</strong></td>
<td></td>
</tr>
<tr>
<td>- Lower intrinsic Capacitance</td>
<td>Low Vdd, but inherently higher than FDSOI</td>
</tr>
<tr>
<td>- Lower intrinsic variability</td>
<td>- 3D architecture required for electrostatics</td>
</tr>
<tr>
<td>- Superior Weff tuning for low power</td>
<td></td>
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<tr>
<td>- Forward body-bias</td>
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</tbody>
</table>
Scaling rules down to 7nm node

TCAD with Electrostatic considerations

![Graph showing scaling rules down to 7nm node](image)

Required TSOI (nm)

TSOI (thick BOX=145nm)
TSOI (UTBOX case)

NanoWire

TBOX= 25nm
10nm
7.5nm
25nm
TBOX= 145nm

DIBL=100mV/V

5nm Tsi

Courtesy of CEA-LETI, O. Faynot et. al. IEDM 2010
22FDX™: The Right Technology at the Right Time

Server

High Performance Computing & Switching

28HPP

14LPP/LPE

10/7nm

High-end Mobile Application Processor

28SLP

22FDX

Wired Networking, Consumer Applications Mid-Range Smartphone

IoT, Wearables, Sensors, Low-end Smartphone

22FDX™ Design Kits available NOW

Next node Target: 10nm FinFET Performance at 20-30% lower die-cost
**22FDX™:** Accelerates Innovation across a wide range of Applications

- **Consumer** (STB/DTV)
  - Beats Energy Star goals and enables small form factors

- **Wearables**
  - Longer battery life and RF integration to reduce system cost

- **IoT/Industrial** (MPU, ISP, MCU)
  - HD image/video, integrated RF/MRAM, battery operation

- **Mainstream Mobile**
  - Meets display, video, and wireless needs w/o FinFET cost

- **Auto/Info-**
  - Lower $T_j$ at 125°C ambient and better Soft Error Rate (SER)

- **WiFi/RF**
  - Achieves higher data rates at lower power
GLOBALFOUNDRIES Technologies & Solutions

MARKETS / APPLICATIONS
- Mobile Computing
- IoT
- Mission Critical

INTERNET BACKHAUL
- Wired / Wireless
- 1G, 2G, 3G, 4G, 5G

DATA CENTERS
- Compute / Clouds

GLOBALFOUNDRIES Technologies & Solutions

FD-SOI
MRAM
RF-SOI & SiGe
SiPh
FinFET

ADVANCED PACKAGING
ASIC

From Sensors to Servers

GLOBALFOUNDRIES Proprietary
Enabling Next Generation Product Innovation with 22FDX™

- 0.4 Volt Operation offers the best energy efficiency
- Software-controlled transistor body-biasing enables Innovative Power Management schemes
- Integrated eNVM and RF enables lowest cost and smallest form-factor
- Post-Silicon Tuning/Trimming enables differentiation
- FinFET-like performance at 28nm-like cost

22FDX™: The Right Technology at the Right Time

Design Kits available now

Let us Lead the next wave of Innovations together!!
Thank you
22FDX™: Multiple Body-Bias and Vt Points on Same Die
Innovative Power Management in Real-time Applications

Integrated RF

Wakes up comm block to transmit message

RBB for lowest leakage

Detects motion

FBB for lowest dynamic power

Wakes up Image Processor to zoom in and analyze

FD-SOI Delivers:

- Low static and dynamic power
- RF integration for reduced BOM cost
- RBB and FBB for power/perf tradeoffs