INVECAS IP Portfolio in 22FDX™

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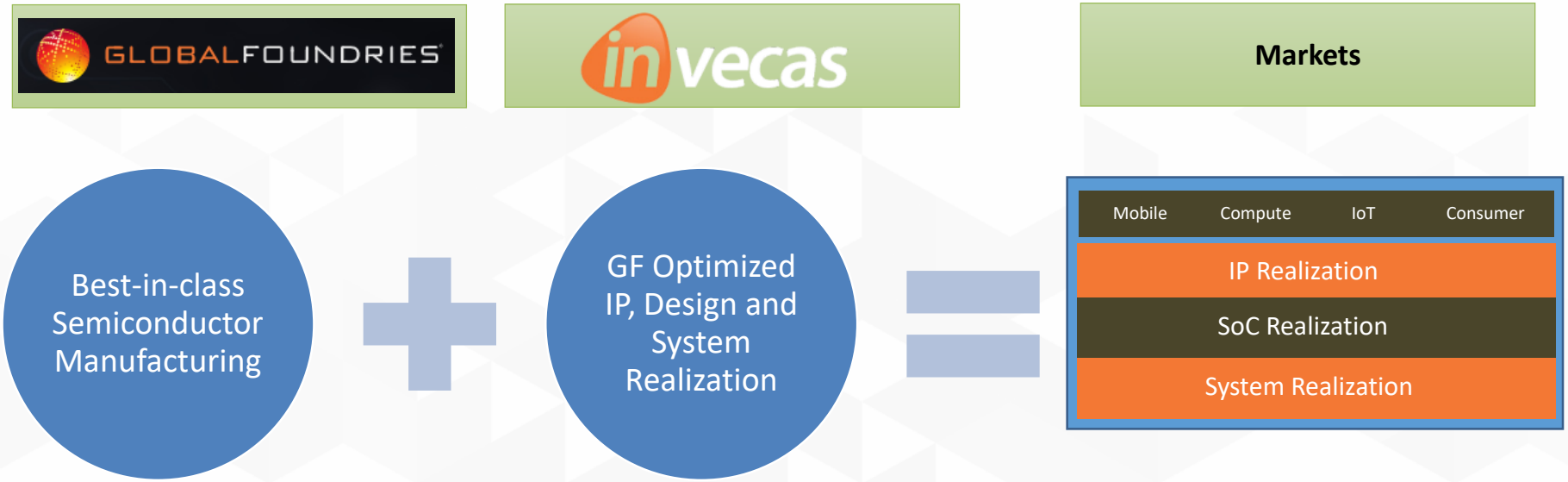
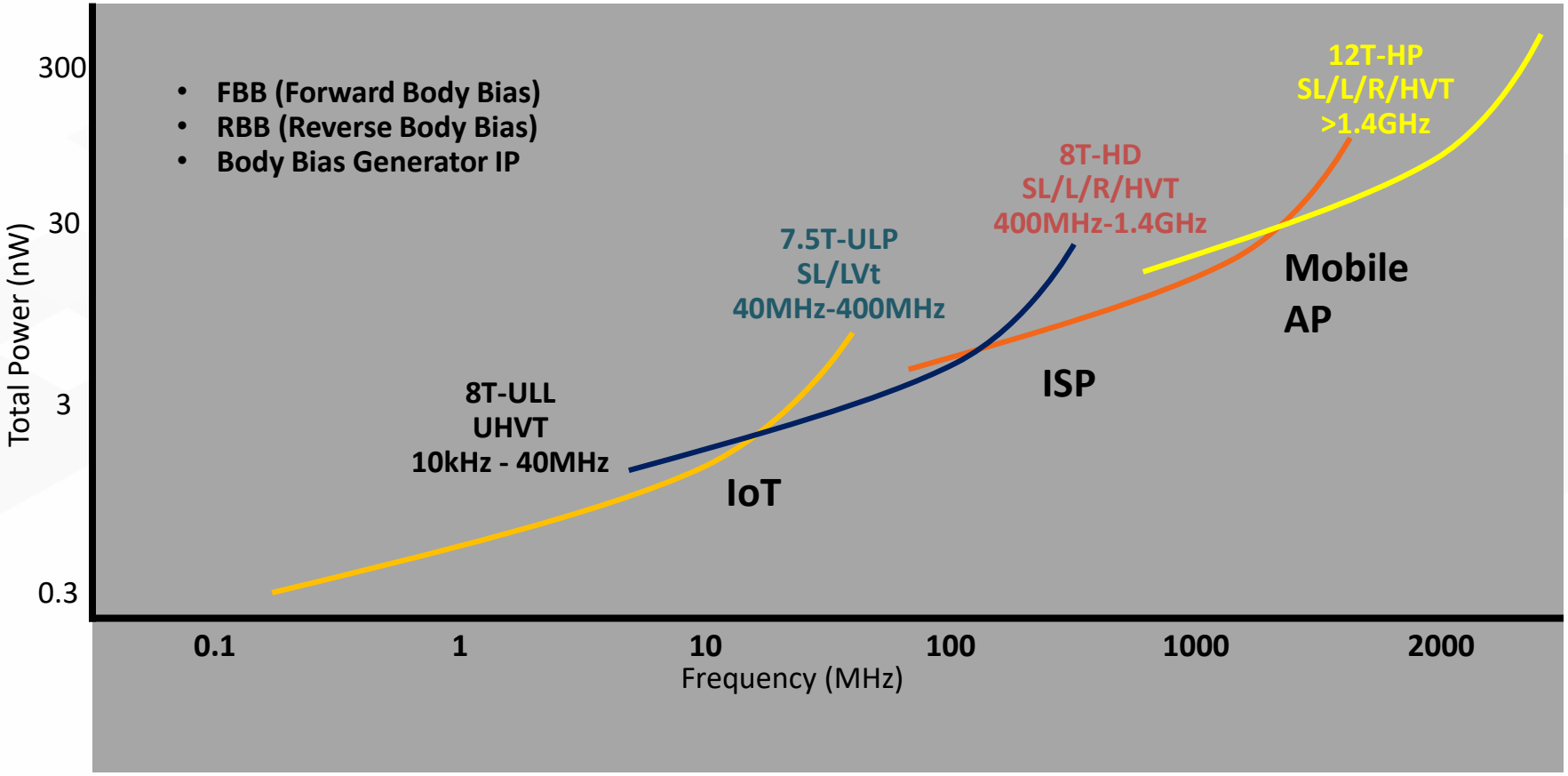
INVECAS and GLOBALFOUNDRIES Strategic Partnership



Broad Range of Standard Cell Libraries to Meet Customer Requirements



Foundation IP – Standard cells

IP Description	Vts	Voltage	Back Bias	Channel Lengths
Low Power 116CPP 7.5T CNRX/SDB Library (ULP)	SLVT/LVT	LVT 0.65v, 0.8v SLVT 0.5v,0.65v, 0.8v	Non Bias	C28, C32, C36
Low Leakage 116CPP Dense 8T ULL Library	uHVT	0.8v		C28, C32, C36
Dense 104CPP Dense 8T CNRX/SDB	SLVT/LVT	0.65v, 0.8v ,0.9v		C20, C24, C28
Performance 104CPP 12T CNRX/SDB	SLVT/LVT	0.8v		C20, C24, C28

Low Power 116CPP 7.5T CNRX/SDB Library (ULP)	SLVT/LVT	LVT 0.65v, 0.8v SLVT 0.5v,0.65v, 0.8v	Bias	C28, C32, C36
Dense 104CPP Dense 8T CNRX/SDB	SLVT/LVT	0.65v, 0.8v		C20, C24, C28
Performance 104CPP 12T CNRX/SDB	SLVT/LVT	0.8v		C20, C24, C28

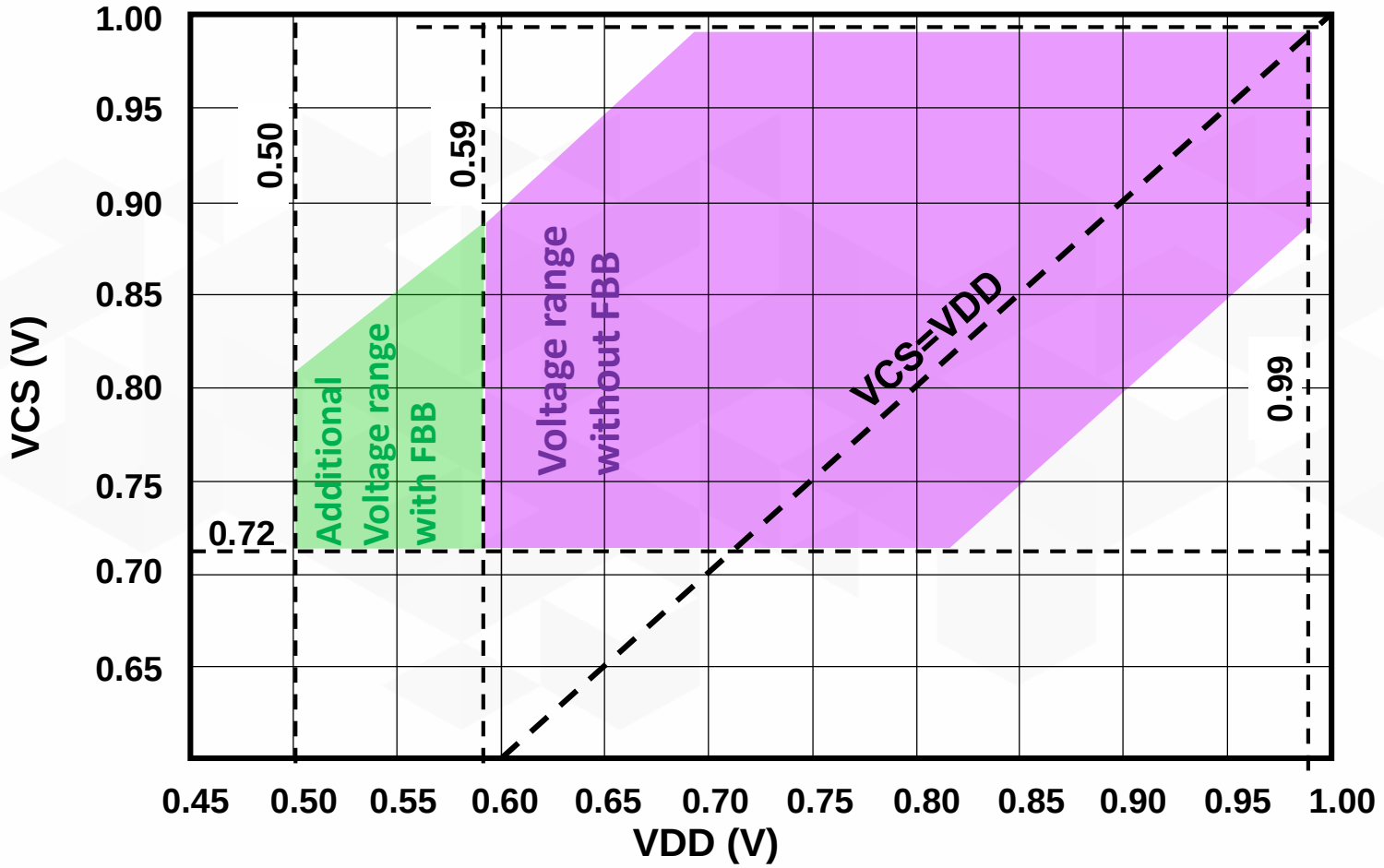
Dense 104CPP Dense 8T CNRX/SDB	RVT/HVT	0.8v	Non Bias	C20, C24, C28
Performance 104CPP 12T CNRX/SDB	RVT/HVT	0.8v		C20, C24, C28

Foundation IP – Memories

IP Description	Supply Voltage
High Performance Memories (800Mhz+)	
High Density Single-Port SRAM , HPP (S1D)	Dual Rail: VCS:0.8v Vdd: 0.8v, 0.65v
High Performance Single-Port SRAM, HPP (S1P)	
High Performance Time-Multiplexed Pseudo Dual-Port SRAM, HPP (SMP)	
High Performance Two-Port Register Files , HPP (R2P)	
Via ROM , HPP (ROMI)	
High Performance Single-Port Register Files, HPP (R1P)	
High Performance Single-Port Register Files , UHPP (R1PH)	Single Rail: VCS=Vdd; 0.9v, 0.8v
Base Memories (300Mhz--800Mhz)	
High Density Single-Port SRAM (S1DV)	Dual Rail: VCS:0.8v Vdd: 0.8v, 0.65v
High Performance Single-Port SRAM (S1PV)	
High Performance Time-multiplexed Pseudo Dual-Port SRAM (SMPV)	
High Performance Single-Port Register File (R1PV)	
High Performance Two-Port Register File (R2PV)	
Dual Port SRAM (SDPV)	
Ultra Low Power Memories (40Mhz - 300Mhz)	
High Density Single-Port SRAM, ULPP (S1DU)	Dual Rail: VCS:0.8v Vdd: 0.8v, 0.65v
High Performance Single-Port Register File, ULPP(R1PU)	
High Performance Two-Port Register File, ULPP (R2PU)	
Via ROM, ULPP (ROMIU)	
Ultra Low Leakage Memories (32Khz – 40Mhz)	
ULL Single-Port SRAM, ULPP (S1C)	Single Rail: VCS=Vdd; 0.8v

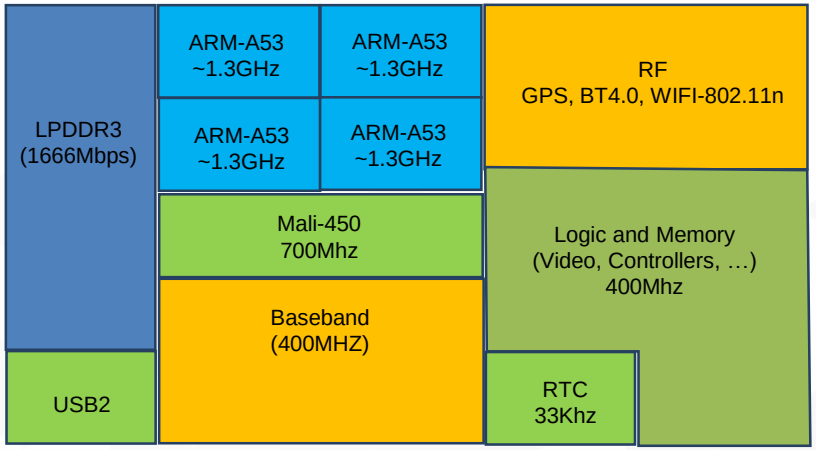
Memories Dual-Supply and FBB Advantage

- Separating Array supply (VCS) with periphery (VDD) allows significant VDD scaling, specially with FBB



Customer Use Case 1

Mobility Block Diagram



SOC Sub-System	Logic Library Options
RTC	8T-ULL @ 0.8v
LPDDR3	8T-104CPP - LVT @ 0.8v - RVT/HVT @ 0.8v
ARM A53	
Mali-450	Single Voltage Domain Option - 8T-104CPP (HVT/RVT) @ 0.8v
Baseband	
Logic & Memory	

Customer Requirements

Voltage Domains: Single 0.8v domain

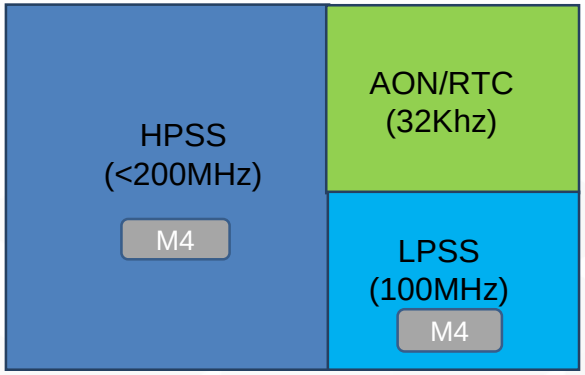
Frequency Modes: No DVFS. Will not use Vt scaling.

PPA

- **Area:** 20% area reduction over 28nm Bulk Process

Customer Use Case 2

High-Level IOT Product Scope



IOT SOC Sub-System	
AON/RTC	8T-ULL @ 0.8vnom
HPSS/ LPSS	SRAM: ULP (Dual-Rail) - VCS: 0.8vnon (0.72vmin) - VDD: 0.65nom (0.59vmin) Logic: Option 1: 0.65vnom

Customer Requirements

Voltage Domains: Multiple

Frequency Modes: DVFS and Vt scaling

PPA

- **Leakage:** 50% less than 40nm Ultra Low Power Process
- **Dynamic:** 30%+ less than 28nm
- **Area:** 20% less than 28nm Bulk Process

Analog and IO IP

IP Type	IP Description
General Purpose and Specialty IO	Voltages 1.2 – 1.8V
	3.3V and interfaces (SPI, I2C, SDIO, eMMC5.1)
	LVDS Tx/Rx
	5V Tolerant Fail Safe IO
Body Bias Generator	Negative / Positive Bias Generators
PLL	Low Jitter General Purpose : 3200 Mhz
Fractional PLL	4500 Mhz
Process Monitor / Temperature Sensor	+/- 1.5 C
Video DAC	3 Channel 10-bit 150MHz
	1 Channel 10 bit 150Mhz
	3 Channel 12-bit 150Mhz
	1 channel 12-bit 150Mhz
Audio CODEC	2 channel 16-bit
	24 bit Audio ADC, 24 bit Audio DAC

Interface IP

IP Type	IP Description
Serdes	1 - 8G Multi Protocol : PCIe – 1.1/2/3, USB 3.0, SATA 1/2/3
	1 – 12.5G Multi Protocol : PCIe – 1.1/2/3, USB 3.0/3.1, SATA 1/2/3, 10G-KR
	1 – 25G Multi Protcol: PCIe – 1.1/2/3/4, USB 3.0/3.1, SATA 1/2/3, 10G-KR, PCIe4- ESM/CCIX
DDR/LPDDR	LPDDR3 : 1600 Mbps
	LPDDDR34 : 4266 Mbps
	LPDDR4/4X : 4266 Mbps
	DDR34/LPDDR34 : 3200 Mbps
MIPI	MIPI MPHY (SSIC/UFS2) with Gear3 support (11.6 Mbps)
	MIPI DPHY 2.5G CSI/DSI
USB2 PHY	USB2.0 OTG, Type-C, BC1.2
HDMI	2.0 Tx (6Gbps)
	2.0 Rx (6Gbps)
Display Port*	1.4 Tx (8.1Gbps)
	1.4 Rx (8.1Gbps)

*In partnership with a third party IP vendor

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