I-fuse™:
Best OTP for FD-SOI and Sub-14nm

Shine Chung, Chairman
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About Attopsemi

- Founded in June 2010
  - By a team of semiconductor veterans and experts
- Located at Si-Soft Research Center of Hsinchu Science Park, Taiwan
- Biz: OTP (One-Time Programmable) IP development and licensing
  - Foundry independent OTP; no additional masks or process steps
  - Program not by NVM ways: blow fuse, rupture oxide or trap charges
  - But by “true electromigration: accelerating wear-out of logic devices”
    - 100x reliability, 1/100 cell size, and 1/10 program current of eFuse
    - Pass HTS at 300°C for 4,290hr; defect rate <0.01ppm
  - Universal and proven OTP from 0.7um to 22nm and 7nm and beyond
- Patent portfolio: >65 filed in US and 11 in Taiwan/China
- Engaged >5 foundries and >50 customers worldwide
The Team

- **Founder**: Shine Chung
  - Harvard graduate in Applied Physics
  - 30 years of IC design experience
  - Memory design in AMD, Intel, and HP
  - PA-WW architect (PA-WW: precedent of Intel’s Merced)
  - Director at TSMC (eFuse pioneer)
  - VLSI and ISSCC technical committee for 4 years
  - Two-time TSMC innovation award recipient
  - More than 61 US patents granted before Attopsemi
  - Filed more than 65 U.S. patents at Attopsemi Technology

- **Co-founder & VP of Eng**: WK Fang
  - MSEE from Ann Harbor, U. of Michigan
  - 20-year experiences in memory
  - Technical Manager at TSMC
  - Department Mgr for eFuse
  - Design managers for N90/N65 SRAM TV, eDRAM
  - MTS in SRAM, FIFO, CAM at IDT
OTP Applications

- OTP: One-Time-Programmable Memory
- Programmable only once to store permanent data
- Allows each IC to be customized after fabrication, no costs
  - Every chip needs OTP, if available, affordable, & reliable

Product feature selection

3D IC repair
Memory repair (replace laser fuse)

MCU code storage (replace flash)

Device trimming / calibration (eliminate EEPROM)

Chip ID, Security Key, IoT
Different OTP Technologies

- **Store data Permanently**
  - NVM device

- **NVM mechanisms**
  - Break fuse, Rupture oxide, or trap charges in floating gates

- **NVM reliability**
  - 10x to 100x lower than logic devices

![Diagram showing eFuse, Oxide rupture, and Floating-gate]

- Break fuse
- Explosive
- ≤ 0.18um
- Grow back
- 29ppm defect

- Rupture oxide
- Explosive
- ≤ 0.18um
- Soft breakdown
- 10ppm defect

- Trap charges
- Statistical
- ≥ 0.35um, ≤ 0.6um
- data retention
- 100ppm defect

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3rd Annual Tokyo SOI Workshop, May 31th-June 1st, 2017
Issues about eFuse

- **Electrical Fuse (eFuse):** most popular OTP technology, but:
- Why is eFuse cell so huge?
- Why post-program fuse resistance distributes so widely?
- Why fuses show diff. types of damage?
- Why defect can’t be lower than 10ppm?
- **Goals:** 100x reliability, 1/100 size, 1/10 program current

1R1T Cell: ~50um² for all nodes

Debris

Defect: 29ppm

E-fuse

Electro-migration

Rupture

Melt

3rd Annual Tokyo SOI Workshop, May 31th-June 1st, 2017
I-Fuse™: OTP of Choice

- 1R1D(P+/NW diode), NOT 1R1T cell
  - Diode delivers 5-6x current with 1/5-1/6 of area
  - => 1/25-1/36 size of e-fuse from IDMs
  - => 1/100 cell size of e-fuse from foundries

- Program current less than \( I_{\text{crit}} \):
  - Control programming vs. explosion
    - => \textcolor{red}{100x reliability}; easy to qualified
    - \(\sim\)100% pgm yield => pre-program fab defects
    - Defect:<1E-8 (I-fuse); ~1E-6 (e-fuse)
  - Proprietary fuse to increase program window

- Small fuse and selector
  - Small size=>heat loss \(\downarrow\) =>pgm eff \(\uparrow\)
    - And lesser program current than \( I_{\text{crit}} \)
      => Need only \(1/10\) of program current
  - 7.5mA@0.18(I-fuse) vs. 18mA@N90(e-fuse)

7.5mA@0.18(I-fuse) vs. 18mA@N90(e-fuse)
What’s I-fuse™ vs eFuse?

- **Non-breaking fuse**: Program below a critical current $I_{\text{crit}}$* and above electromigration (EM) threshold*
- **Deterministic programming**
- => **ultra-high reliability**

- **Breaking fuse**: Program beyond a critical current
- **Explosive programming**
- => **debris grow back**

*US patents granted

Figure 3. I-V characteristics of a typical element upon programming.

**Intel**: IEDM 1997, pp.855

**Attopsemi**: ICMTS 2016, pp148

Figure 3. I-V characteristics of a typical element upon programming.

Intel: IEDM 1997, pp.855

Attopsemi: ICMTS 2016, pp148

Any Power Devices would prevent operating under “thermal run away.” Why a fuse under such condition can be reliable?
Why Non-breaking Fuse?

- Many advantages for non-breaking fuses:
  - => low program voltage => No charge pump requirement
  - => Uses standard logic design/test flow
  - => low program current => smaller size
  - => lower power
  - => control program => tight fuse resistance distribution
  - => higher reliability
  - => less damage => sustain high temperature
  - => higher data security
  - => electro-migration => no debris after program => no grow back

- Applications:
  - Low voltage/current program/read: 0.7um to 14/10/7nm
  - High quality, reliability: IoT, Automotive, Industry, communication

Only OTP programming mechanism that can be modeled by physics: heat generation/dissipation and electro-migration
300°C 4Khr I-Fuse™ Bake

- We made OTP history: the only OTP passes HTS 300°C, 4,290hr
- 96 dies of 4Kx8 (3Mb I-fuse™) at 0.16um HV pass HTS 300°C, 4Khr
  - No defect found and no redundancy
- Cell current variation after stress vs. before stress
  - Cell current changes <5% after baking
400°C 8hr I-Fuse™ Bake

- I-fuse™ cell current variation <5% after HTS 400°C for 8hrs
  - Passing 400°C for >2hr is a must in RDL process for 3D IC
  - Foundry eFuse can’t pass 400°C for 2hrs, with 20-30 defects in 1Mb
  - 96 4Kx8 I-fuse™ dies @0.16um HV passed @400°C (0 defects in 3Mb)
I-Fuse™: Qual Status

- Vanguard International

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<th>Item</th>
<th>Geometry</th>
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<th>Config.</th>
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- Qual’d by many companies in US, Europe, Japan, Korea, Taiwan, and China, in elevated temperature

- Volume productions in consumer and automotive ICs
Why FD-SOI?

- Want a phone as small as a watch?
- You need FD-SOI
  - RF integration (multi-band/mode)
  - Small form-factor
  - Ultra-low power (e.g. 0.4V/1uA)
  - Low costs
Beyond 10/7nm: Anti-Fuse (AF)

- Junction breakdown (BVJ) lowers than oxide (BVO) to work
- Oxide can’t be scaled => program voltage can’t be lower
  - PGM Voltage: 7.0V@0.18, 6.5V@40nm, and 4.5V@28nm
- Junction breakdown decreases for sub-14nm: eSiGe, cSiGe
- FD-SOI has much lower junction breakdown than bulk

![Graph showing BVJ/BVO breakdown voltage of junction/oxide](image)
Beyond 10/7nm: I-Fuse™

- I-fuse™ proven from 0.7um to 22nm and soon to 7nm
- Programming current scaled with shrinking feature width
- So is the program voltage
- I-fuse™ @22nm FD-SOI: PGM voltage <1.0V with 1/20 area than AF

For FD-SOI and sub-14nm:
I-fuse™ current programming prevails AF voltage programming !!!

![Graph showing I_crit vs Lg with data points]
IoT Is Data Security

Which I-fuse™ at GF 28nm has been programmed?

Heck a fuse 90%, hack 1Kb ~ 0 \((0.9^{1.000}=1.39E-47)\)!!
I-Fuse™: ZERO Defect

- Field return is very costly
  - 10x costs from wafer sort, packaged chip, module, PCB, to system
- ZERO defect after shipping
  - Defects should be found out and screened before shipping
- I-fuse™ can achieve ZERO defect
  - OTP dilemma: fully tested before shipping; can’t be used after tests
  - Guarantee programmable: if initial fuse resistance <400Ω
  - Guarantee 100% programmable: if program within specs
  - Fully testable: every functional block, including program circuits
I-Fuse™ for IoT

- **Internet-of-Things (IoT)**
  - Low cost, low power wireless sensor network
  - 30B internet-enabled device by 2020--- 3-5x market of smart phone
  - FD-SOI is the ideal CMOS technology for IoT

- **I-fuse™ for IoT**
  - Low voltage: I-fuse™ program voltage at 1.0V
  - Low current: I-fuse™ read voltage at 0.4V, current at 1uA
  - High data security: I-fuse™ program state undetectable
**I-Fuse™ for 3D IC**

- **3D IC**
  - Stacking 20-30 dies by interposer or Through Silicon Via (TSV)
  - Only way to extend Moore’s law: low power & high integration

- **I-fuse™ for 3D IC: I-fuse™ in every die stacked**
  - I-fuse™: allow repairing heterogeneous dies from 0.5um to 7nm
  - I-fuse™: pass 400°C >2hr Redistribution Layer (RDL) process in 3D IC
  - I-fuse™: guarantee ZERO defect in programming => no field return
  - I-fuse™: Post-package programming without charge pumps
Conclusions

• **I-fuse™**: a proven OTP technology
  - Many customers in volume productions

• **I-fuse™**: the OTP of choice
  - Scalable: from 0.7um to 7nm and beyond
  - *Especially for SOI*: much lower device breakdown voltage
  - High reliability: *ZERO* defect => guarantee no field return
  - High temperature: from -55°C to 200°C
  - Small size: up to 1/100 of eFuse, smaller than anti-fuse
  - Low program voltage: based on I/O voltages (w/o charge pumps)
  - High data security: program status is undetectable

• **I-fuse™** enable new OTP applications
  - IoT: low cost, low power, and high reliability wireless sensor network
  - Automotive: qual passed 250oC for 1K hrs
  - 3D IC repair: allow heterogeneous dies from diff. foundries repaired

• **Call for participation to become industry standard**
  - High quality, high reliability, and save costs
Myths about OTP

- OTP market size too small
  - All chips need OTP
  - 1% of royalty for $300B worldwide market means $3B
  - Majority of OTP in use are in-house eFuse
- OTP is an NVM memory and should be qual’d like an NVM
  - Existing OTPs are NVMs: break fuse, rupture oxide, & trapping charges
  - Innovative I-fuse(tm) OTP: non-breaking fuse: a logic device
- Conventional eFuse programming is based on electromigration (EM)
  - A mixed of EM/rupture/decompose/melt under thermal runaway
- Breaking a fuse is more reliable
  - Breaking a fuse by explosion ISN’T; Raising fuse resistance by EM IS
- High post- and pre-program fuse resistance ratio is a figure of merit
  - 5X or 10X resistance ratio is good enough for sensing
- OTP needs redundancy
  - OTP should have high yield and high reliability. Needs no redundancy