Analog/RF design techniques in 28nm FD-SOI technology

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Fully depleted Silicon-on-Insulator (FD-SOI)

- **Power and energy efficiency**
- **Analog performance** for mixed signal and RF design
- **Robustness** for mission critical applications

FD-SOI is unmatched for **cost-sensitive** markets requiring digital and Mixed Signal SoC **integration and performance**
ST 28nm FD-SOI Transistor Flavors

Low VT (LVT) CMOS in FD-SOI; flipped-well

Regular VT (RVT) CMOS in FD-SOI

Bulk type CMOS
### FD-SOI for Simpler Analog Integration

ST 28nm FD-SOI makes analog/RF/HS designer’s life easier

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefits</th>
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<tbody>
<tr>
<td>Improved Analog Performance</td>
<td>Speed increase in all analog blocks</td>
</tr>
<tr>
<td></td>
<td>Higher gain for a given current density</td>
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<tr>
<td>Improved Noise</td>
<td>Lower gate and parasitic capacitance</td>
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<td>Lower noise variability</td>
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<tr>
<td>Efficient Short Devices</td>
<td>Better matching for short devices and efficient design with ( L &gt; L_{\text{min}} )</td>
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<tr>
<td>Very large ( V_T ) tuning range</td>
<td>Analog parameters wide range tuning via a new independent “tuning knob” (back-gate)</td>
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<td>High performance frequency behavior</td>
<td>( f_T / f_{\text{max}} &gt; 300 \text{GHz} ) for LVTMOS and high performance passives enabling RF/mmW/HS integration with technology margin</td>
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Higher bandwidth
Lower power
Smaller designs
Improved design margins wrt PVT variations
Novel flexible design architectures
Advantages in Analog Design

Efficient Short Devices
- Efficient use of short devices:
  - High analogue gain @ Low L
  - Low Vt mismatch (Avt ~ 2mV.µm)
- Performance example:
  - A 1µm/100nm device has a DC gain of 80 & a Vt of only 6mV

Improved Analog Perf.
- Higher Gm for a given current density
- Lower gate capacitance
  Higher achievable bandwidth or lower power for a given bandwidth

Improved Noise
- For NLVT MOS 1µm/120nm @ 1µA drain current, get 1.5dB lower 1/f noise in FDSOI
Advantages in Analog Design-II

- **Flip-well devices:**
  - Large Forward Body Bias (FBB) range
  - Negligible control current

- **Use back-gate as « VT tuning knob »:**
  - Unprecedented ~250mV of tuning range for FD-SOI vs.
  - ~ 10’s mV in any bulk
Advantages in RF/mmW Design

Active devices high frequency performance

• For ST 28nm FD-SOI LVTNFET: \( f_T / f_{\text{max}} > 300\text{GHz} \)

• For RF operation frequency:
  - Work with \( L = 100\text{nm} \)
  - MAG = 12dB @10GHz
  - NFmin \sim 0.5dB @ 10GHz
  - Work @ current density: 125 \( \mu\text{A}/\mu\text{m} \)

• For mmW operation frequency (intrinsic models):
  - Work @ \( L_{\text{min}} \)
  - MAG = 12dB @60GHz
  - NFmin \sim 1.3dB @ 60GHz
  - Work @ current density: 200 \( \mu\text{A}/\mu\text{m} \) \( \Rightarrow \) 33% less power than in 28LP bulk

Performant passive devices

• Few passive devices examples:
  - Inductor \( L=0.5\text{nH} \) \( Q=18 \) @10GHz, 8ML
  - Varactor \( C=50\text{fF} \) \( Q=20 \) @20GHz
  - Tline: 0.8dB/mm @60GHz \( Z_c=50 \) Ohm, 8ML
Example of mmW- full BEOL implementation of RF transistor

- Starting from Design Kit Pcell (up to M1):
  - compliant with EM current density requirements @110°C
  - minimize transistor $f_t/f_{max}$ degradation:
    - Thin stair-case accesses for low fringe parasitic capacitors between drain and source and minimize parasitics to gate
    - Dual gate access for improving gate resistance

**NLVT MOS in 10ML BEOL**

- $L = 30\text{nm}$
- $W_{\text{finger}} = 800\text{nm}$
- $W_{\text{total}} = 16\mu\text{m}$
- $N_{\text{fingers}} = 20$
- $I_{\text{drain}} = 5.2\text{mA}$

<table>
<thead>
<tr>
<th></th>
<th>Simulation PCell</th>
<th>Simulation Pcell + Back End</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_T$</td>
<td>295 GHz</td>
<td>253 GHz</td>
<td>246 GHz</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>394 GHz</td>
<td>370 GHz</td>
<td>359 GHz</td>
</tr>
</tbody>
</table>

Nota: on-wafer measurements with classical pads and access de-embedding method; Measurements performed on 10-110GHz and 220-330GHz test benches independently

[R. Guillaume at al, RFIC2017]
Advantages in Mixed Signal Design

- Tighter process corners and less random mismatch than competing processes

- Benefits:
  - Simpler design process, shorter design cycle
  - Improved yield or improved performance at given yield

Variability

- Improved gate control allows smaller VTH
- Backgate bias allows for VTH reduction by tuning
- Results is an unprecedented quality of analog switches
- Compounding benefits: smaller R -> smaller switch -> compact layout -> lower parastics -> even smaller switch
- Key for high performance data converters and other Switched-Cap. Circuits

Switch performance

- Lower junction capacitance makes a substantial difference in high-speed circuits
  - Drastic reduction of self-loading in gain stages
  - Drastic reduction of switch self-loading

- Two-fold benefit:
  - Leads to incremental improvements
  - Allows the designer to use circuit architectures that would be infeasible/inefficient in bulk technologies

Lower capacitance

- 28FDSOI vs 28lp bulk

Vth (mV)

Gate length (m)
« Front side » transistor parameters monitoring for Vbody variation (measured data)

- DC data, Gm vs ids
  - Vbody = 0…2V
  - Vds = 1.1V

- RF data @ 10GHz, Gm vs ids
  - Vbody = 0…2V
  - Nfingers = 20

- RF data* @ 10GHz, f_T vs ids
  - Vbody = 0…2V
  - Nfingers = 20
  - *: intrinsic device (Pcell)

- Vbody has no impact on « front-side » transistor parameters (Gm, f_T), at a given drain current
FD-SOI electrical models and implementation in 28FDSOI DP
Leti-UTSOI: a $\Psi_S$ compact model based on PSP model for SOI

- SOI device physics imply taking into consideration new phenomena:
  - Interface coupling, does not exist in bulk
  - new drain-source currents distribution; gate to bulk tunneling current does not exists in SOI
  - Short channel effect: bulk type charge sharing is replaced by 2D electrostatic behavior
  - Self heating effect; negligible in bulk

- The Leti-UTSOI2 model:
  - a surface potential compact model including the bottom interface inversion (thin buried oxide with non-zero substrate bias)
LETI-UTSOI2 model well captures all the effects due to inversion channel formation at the SOI back interface in Forward Body Bias (Vb>0) regime, both in DC and AC.
RF subcircuit

**Leti-UTSOI 2 takes into consideration:**
- Intrinsic charges (Cox, Cinv, Cbox)
- Id, Ig
- Source/Drain access resistances
- Parasitic capacitances: Cfr, Cgbov

**RF Model Extension:**
- Rg, gate resistance model
- Cfr, fringing cap from MEOL
- Cgb
- complete Back-Gate network adding NWELL/PWELL-PSUB junctions

[JC Barbé et al, RFIC2015]
Maximum measured values for front-gate 28nm FDSOI transistors:
- Max($f_T$) = 384GHz
- Max($f_{max}$) = 392GHz
$f_T$ and $f_{\text{max}}$ for back-gate measurements vs simulations with Leti-UTSOI2

Maximum measured values for back-gate 28nm FDSOI transistors:
- $\text{Max}(f_T) = 72\, \text{GHz}$
- $\text{Max}(f_{\text{max}}) = 38\, \text{GHz}$
Overview of RF MOS model offer

- RF MOS transistors are generally dedicated devices in PDK

- Linked to a dedicated Pcell for layout
  - With sufficient tunable parameters allowing optimization for a given application

- Described using dedicated RF models
  - Derived from S-parameter and Noise Figure measurements
  - Featuring all relevant R and C parasitics

- Modeling of Non-Quasi Static effects is a plus
RF MOS PCell general features

• Handle layers up to Metal1 only
  • Consistent with parasitic elements included in the model

• Access to front gate
  • As small as possible poly head(s)
  • Poly head(s) can have 1 or 2 contact rows
  • Front gate can be connected on both sides

• Flexible topology for Source/Drain accesses
  • Inner Source/Drain can have 1 or 2 contact rows
  • Variable number of contacts per row
  • Variable distance of contacts to poly

• Access to back-gate (well strap) is always drawn
  • Allow accurate modeling of back-gate impedance
  • Need to keep layout flexible for well strap
RF MOS PCell-based layout examples
RF modeling of back-gate access
Non Quasi-Static (NQS) modeling

- Can be achieved using MOS transistor channel segmentation

- Channel segmentation features
  - 5 segments are enough to capture NQS frequency dependence up to 10x $F_t$
  - Each segment consists of an intrinsic MOS transistor model instance
  - Extrinsic parasitic elements are accounted for in a sixth transistor model instance
NQS modeling of MOS trans-conductance vs. frequency

Quasi-Static RF model

Non Quasi-Static RF model

NMOS, W = 1µm, L=1µm, V_{gs}=0.8V
Analog/RF/mmW Design examples in FD-SOI
- on the usage of body biasing
From bloc level to system level and SoC
Body biasing techniques for analog/MS/RF designs

• Take advantage of the unique very wide-band body biasing (BB) voltage range
• Propose unique techniques bringing uncontested chip energy saving and revisiting performances SoA

**Method 1:** BB voltage variable over time and PVT
  • Cancel system level PVT effects by continuously tuning transistors’ respective $V_T$
    • Design examples: J. Lechevalier ISSCC2015, D. Danilovic RFIC2016, G. De Streel VLSI2016, R. Guillaume RFIC2017
  • Reconfigure circuit/bloc/system depending on application operation mode
    • Design examples: A. Larie ISSCC2015 (bloc level), G. De Streel VLSI2016 (system level)
  • Propose new energy efficient design techniques for tunable blocs via body tie
    • Design examples: I. Sourikopoulos ESSCIRC2016

**Method 2:** fixed BB voltage
  • Enable operation at ULV (0.5V) and in the same time increase circuit speed
    • Design examples: L. Fanori RFIC2015, A. Lahiri ESSCIRC2016
  • Minimize switches $R_{on}$ value and excursion for energy efficient and high speed switched-capacitors circuits (e.g. ADC)
    • Design examples: S. Le Tual ISSCC2014, A. Kumar ESSCIRC2016
  • Non-overlapping clock generation in massively digital RF Receivers, to increase system linearity
    • Design example: R. Kasri CICC2017
Analog Filter Design Example

- Filters with several 100’s MHz bandwidth
  - PVT + ageing affect system operation
  - Need to tune/trim independently several parameters impacting overall system:
    - cut-off frequency,
    - linearity,
    - noise,
    - all for an optimal power consumption

Regular CMOS Tuning/trimming solution: Voltage regulator impacting directly the signal path behavior

FD-SOI revolutionary solution: individual transistors body biasing oxide-isolated from the signal path behavior
Typical example of Analog Filter

- Inverter-based analog functions:
  - attractive implementations: simple and compact
  - scale nicely with technology nodes
- Here: analog low-pass Gm-C filter
- Typical implementation:
  - Fixed capacitors
  - Tune the filter cut-off frequency by tuning Gm

Bulk specific solution: Tune local Vdd
FD-SOI specific solution: Tune all VBB’s
Tuning Gm with $V_{DD}$

**OK**: gm variation; **NOK**: linearity

- Tune Gm value with local VDD
- Major issue: it changes also linearity and noise behavior
FD-SOI: Tuning gm with Vbody

OK: gm variation; OK: linearity

• New tuning knob (and off the signal path): VBBP and VBBN

• Compensate $V_{DD}$ variations
  • Tune gm back to nominal
  • Ensure constant linearity operation

Without back-gate bias

With back-gate bias
Inverter-based Analog Filter in 28FDSOI

- RF low-pass Gm-C filter using CMOS inverters
  - Tuned by back-gate instead of supply (no signal path interference) \(\Rightarrow\) enabled by FDSOI
  - Supply regulator-free operation
    - Energy efficient
    - Low voltage operation (VDD = 0.7V)
    - Competitive linearity
- Compared to similar circuit in 65nm bulk [2], at same noise level, get X2 linearity for /4 power level
- Compared to best-in-class filters [7], at same noise level and Fc, get competitive linearity for /14 power level
- Best in class in terms of the compromise noise-linearity-power
- Integrated in ST 28nm FD-SOI CMOS

<table>
<thead>
<tr>
<th>Technology</th>
<th>This work</th>
<th>[2]</th>
<th>[5]</th>
<th>[6]</th>
<th>[7]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>28nm FD-SOI CMOS</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>0.13um CMOS</td>
<td>0.18um CMOS</td>
</tr>
<tr>
<td>Order</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>0.7</td>
<td>0.8</td>
<td>3</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>Cut-off freq. [MHz]</td>
<td>454</td>
<td>454</td>
<td>457</td>
<td>459</td>
<td>4700</td>
</tr>
<tr>
<td>Input ref. noise [nVrms/√Hz]</td>
<td>5.9</td>
<td>6.1</td>
<td>6.1</td>
<td>5.9</td>
<td>6.6</td>
</tr>
<tr>
<td>in-band IP3 [dBVp]</td>
<td>1.2</td>
<td>4.0</td>
<td>4.0</td>
<td>2.4</td>
<td>-3</td>
</tr>
<tr>
<td>Power diss. [mW]</td>
<td>4.0</td>
<td>4.6</td>
<td>5.2</td>
<td>5.6</td>
<td>19</td>
</tr>
<tr>
<td>SFD/BW [dB/Hz]</td>
<td>109</td>
<td>110</td>
<td>110</td>
<td>109</td>
<td>105</td>
</tr>
<tr>
<td>NSNR [dB]</td>
<td>137</td>
<td>139</td>
<td>138</td>
<td>137</td>
<td>125</td>
</tr>
</tbody>
</table>

[J. Lechevalier et al, ISSCC2015]

A Low-Power Inductor-less RFFE with IIP2 Callibration for BTLE applications, coexistence with LTE band 7

[D. Danilovic et al., RFIC2016 and NEWCAS2015]

- Compact, energy efficient RF Front-End in 28FDSOI
- System level performance within BT specs with LTE coexistence (IIP2 >70dBm)
- Inductor-less Low Noise Transconductance Amplifier
  - Common gate with cross-coupling caps
  - Complementary NMOS/PMOS
  - Noise Cancellation

- Differential IQ passive mixer with 25% duty cycle
  - Tune switches mismatch through body biasing

- **FDSOI advantages:**
  - LNTA: higher intrinsic gain, less parasitics
  - Huge IIP2 improvement through body-biasing
  - Overall energy efficient design
A Low-Power Inductor-less RFFE with IIP2 Callibration for BTLE applications, coexistence with LTE band 7

- IIP2 measurement results

**Different Blocker Scenarios:**

\[ f_1 = f_{LO} + f_x, \quad f_2 = f_{LO} + f_x + 4\text{MHz} \]

- \( f_x = 40\text{MHz} \): +20dB IIP2 improvement
- \( f_x = 100\text{MHz} \): +25dB IIP2 improvement
- \( f_x = 200\text{MHz} \): +31dB IIP2 improvement

**Different Chips, IIP2 improvement with Body biasing:**

- **Chip1:** +24dB IIP2 improvement
- **Chip2:** +30dB IIP2 improvement
- **Chip3:** +23dB IIP2 improvement

\[ V_B = 1\text{V} \]

\[ V_{Bdiff} = V_{Btune1} - V_{Btune2} \]
A 2.8 to 5.8GHz Harmonic VCO in 28FDSOI

- Very wide Tuning Range to address CA needs
- Reconfigurable active core and tailored 8-shape tank inductor

**FDSOI Technology enablers:**
- Low VT body biased active devices for higher max frequency and tuning range
- High quality passives thanks to the SOI features
- Competitive core area, performance PhN and FOM, rejection of external magnetic fields and producing itself a vanishing magnetic field

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[L. Fanori et al., RFIC2015]
50% power in mmW TRx spent in PA

Solve the general trade-off linearity and power consumption

WiGiG with max. operation probability @ 8dB back-off ➔ high linearity with optimized power
Novel mmW Power Amplifier
thanks to FD-SOI and wide-range body biasing

- Revisit classical Doherty power amplifier architecture
- Two different class power amplifier in parallel
  - Ability of *gradually* change the overall class of the PA (mix of class AB and class C) thanks to wide range FBB → optimise in the same time power efficiency and linearity
- Remove signal path power splitter as in classical implementations → reduced signal path losses
60GHz Configurable PA

- Fully WiGiG compliant (linearity and frequency range)

- **New PA architecture enabled by FDSOI**: continuously reconfigurable power cells

- Continuous operation class tuning thanks to body bias with 2 extreme modes:
  - High gain mode: Highest ITRS FOM
  - **10X better than previous SoA**
  - High linearity mode: Break the linearity / consumption tradeoff

- ULV high efficiency operation (Vdd_min = 0.8V)

- Integrated in ST 28nm FD-SOI CMOS

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### Table

| Technology  | Operating mode | Supply voltage [V] | Frequency [GHz] | Gain [dB] | P$_{\text{SAT}}$ [dBm] | P$_{\text{1dB}}$ [dBm] | PAE$_{\text{max}}$ [%] | PAE$_{\text{1dB}}$ [%] | PAE$_{\text{8dB}}$ [%] | DC [mW] | DC$_{\text{8dB}}$ [mW] | 100xP$_{\text{1dB}}$/P$_{\text{DC}}$ | Active area [mm$^2$] | IT$\text{R}$S FOM [W.GHz$^2$]
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>28nm UTBB FD-SOI</td>
<td>High gain</td>
<td>1.0</td>
<td>61</td>
<td>35</td>
<td>18.9</td>
<td>15.7</td>
<td>17.7</td>
<td>9</td>
<td>1.5</td>
<td>331</td>
<td>332</td>
<td>9.6</td>
<td>0.162</td>
<td>161,671</td>
</tr>
<tr>
<td>28nm UTBB FD-SOI</td>
<td>High linearity</td>
<td>0.8</td>
<td>60</td>
<td>15.4</td>
<td>18.8</td>
<td>21</td>
<td>21</td>
<td>21</td>
<td>8</td>
<td>74</td>
<td>124</td>
<td>89</td>
<td>1,988</td>
<td>1,198</td>
</tr>
<tr>
<td>40nm</td>
<td>Low/High power</td>
<td>0.9</td>
<td>60</td>
<td>15.1</td>
<td>16.9</td>
<td>23</td>
<td>23</td>
<td>23</td>
<td>7.5</td>
<td>58</td>
<td>84</td>
<td>72</td>
<td>1,198</td>
<td>1,198</td>
</tr>
<tr>
<td>40nm</td>
<td>1.0</td>
<td>61</td>
<td>16.8 / 17</td>
<td>12.1 / 17</td>
<td>15.6</td>
<td>22.2 / 30.3</td>
<td>18.9</td>
<td>14.1 / 21.6</td>
<td>3</td>
<td>56 / 75</td>
<td>94</td>
<td>94</td>
<td>1,988</td>
<td>1,198</td>
</tr>
<tr>
<td>40nm</td>
<td>0.9</td>
<td>60</td>
<td>26</td>
<td>16.2</td>
<td>15.6</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>3</td>
<td>56 / 75</td>
<td>94</td>
<td>94</td>
<td>1,988</td>
<td>1,198</td>
</tr>
<tr>
<td>65nm PD-SOI</td>
<td>NA</td>
<td>1.0</td>
<td>60</td>
<td>16</td>
<td>15.6</td>
<td>15.2</td>
<td>12.7</td>
<td>11.1</td>
<td>22.6</td>
<td>77.4</td>
<td>79</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65nm PD-SOI</td>
<td>NA</td>
<td>0.9</td>
<td>16</td>
<td>15.6</td>
<td>15.2</td>
<td>12.7</td>
<td>11.1</td>
<td>22.6</td>
<td>77.4</td>
<td>79</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**ITRS FOM** = $P_{\text{SAT}} \cdot \text{PAE}_{\text{max}} \cdot \text{Gain} \cdot \text{Freq}^2$

*: with pads  #: estimated
A Digital Delay Line with Coarse/Fine tuning through gate/body biasing in 28FDSOI

- Novel low power design architectures for 60GHz receivers enabled by FDSOI: DFE with un-clocked delay feedback, search minimum delay spread at 2GS/s data rate
  - Total delay >10ns
  - Granular delay < 500ps

- FDSOI specific unity delay cell (thyristor revisited):
  - Body bias control for rising/falling edge delay fine tuning
  - Gate control for coarse delay tuning
  - Complementary input scheme for reduced power consumption

- State of the art results: ultra wide range linear control, fs/mV sensitivity and energy efficiency

[I. Sourikopoulos et al., ESSCIRC2016]
mmW Design Example: Distributed Oscillator at 134 GHz

\[ f_{osc} = \frac{1 - \Delta \phi(f) / \pi}{2nl\sqrt{LC}} \]

- The oscillation frequency depends on:
  - The electrical Tline parameters
  - The transistor inverting properties around \( F_{osc} \) (\( F_{max} \))
  - The highest \( F_{osc} \) topology proposed so far in a 28nm node
Distributed Oscillator: Correlation measurements vs simulation

- Oscillation frequency measurements
  - Histogram over 8 locations on a wafer: <0.1% variation simulation vs measurements
  - Very small on wafer dispersion

- Phase noise optimization/tuning/trimming via body biasing

Simulation:
- $f_{osc} = 134.14$ GHz

Theory:
- $f_{osc} = 134.2$ GHz
mmW Distributed Oscillator in 28nm FD-SOI: comparison with the SoA

\[ \text{FoM} = \text{PN (@} f_m,\text{)} - 20 \log \left( \frac{f_0}{f_m} \right) + 10 \log \left( \frac{P_{\text{diss}}}{1mW} \right) \]

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq. (GHz)</th>
<th>Output Power (dBm)</th>
<th>DC-to-RF Efficiency</th>
<th>PN @1MHz (dBc/Hz)</th>
<th>DC Power (mW)</th>
<th>Area (mm²)</th>
<th></th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>121</td>
<td>-3.5</td>
<td>2.07%</td>
<td>-88</td>
<td>21.6</td>
<td>0.135</td>
<td>176.3</td>
<td>130nm CMOS</td>
</tr>
<tr>
<td>[2]</td>
<td>177</td>
<td>3.4*</td>
<td>9.35%*</td>
<td>-105.4*</td>
<td>23.4</td>
<td>0.130</td>
<td>196.7*</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>[3]</td>
<td>210</td>
<td>1.4</td>
<td>2.44%</td>
<td>-87.5</td>
<td>56.5</td>
<td>0.080</td>
<td>176.4</td>
<td>130nm SiGe</td>
</tr>
<tr>
<td>[4]</td>
<td>212</td>
<td>-7.1</td>
<td>0.65%</td>
<td>-92</td>
<td>30</td>
<td>0.073**</td>
<td>183.8</td>
<td>130nm SiGe</td>
</tr>
<tr>
<td>[5]</td>
<td>219</td>
<td>-3</td>
<td>2.09%</td>
<td>-77.4</td>
<td>24</td>
<td>0.105</td>
<td>170.4</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>**</td>
<td><strong>This Work</strong></td>
<td><strong>134.3</strong></td>
<td><strong>5.48% †</strong></td>
<td><strong>-99.6 †</strong></td>
<td><strong>20 †</strong></td>
<td><strong>0.090</strong></td>
<td><strong>188.9 †</strong></td>
<td><strong>28nm CMOS FDSOI</strong></td>
</tr>
<tr>
<td></td>
<td>202.2</td>
<td><strong>0.3 †</strong></td>
<td><strong>5.38% †</strong></td>
<td><strong>-100.4 †</strong></td>
<td><strong>20 †</strong></td>
<td><strong>0.065</strong></td>
<td><strong>193.5 †</strong></td>
<td></td>
</tr>
</tbody>
</table>

(*full transmitter / **Without pads / †at optimum Phase Noise)
A 6b 10GS/s High-Speed Time Interleaved-ADC

- Lower Vth, less variability
- Better switch: $R_{ON}$ & linearity
- Faster logic
- Reduced S/D capacitances
- Increased comparator BW
- Reduced switch parasitics
- Energy efficient operation
- Integrated in ST 28nm FD-SOI CMOS

Verma ISSCC 2013 | Tabasy VLSI 2013 | Kull VLSI 2013 | This Work
--- | --- | --- | ---
Technology | 40nm CMOS | 65nm CMOS | 32nm SOI | 28nm FD-SOI
Architecture | TI-FLASH | TI-SAR | TI-SAR | TI-SAR
Power Supply (V) | 0.9 | 1.1 / 0.9 | 1 | 1
Sampling Rate (GS/s) | 10.3 | 10 | 8.8 | 10
Resolution (bits) | 6 | 6 | 8 | 6
Power Consumption (mW) | 240 | 79.1 | 35 | 32
SNDR @ Nyquist (dB) | 33 | 26 | 38.5 | 33.8
Active Area (mm²) | 0.27 | 0.33 | 0.025 | 0.009
FOM @ Nyquist (fJ/conv) | 700 | 480 | 58 | 81
Max Input Frequency (GHz) | 6 | 4.5 | 4.2 | 20
Gain/Skew Calibration | Yes | Yes | Yes | No

Courtesy, B. Murmann, Stanford Univ.
A Single Channel 12b 600Ms/s ADC with no calibration
- architecture: 2x 2.5b pipeline stages followed by a 8b A-SAR, with no calibration loop

• FBB (± 1.8V)
  - Switch linearity improved by a factor of 40
  - Ron improved by a factor of 5
  - Smaller switches with smaller parasitic cap

• FBB (± 1.8V)
  - 2x logic speed
  - Improved comparator delay
  - Improved linearity and speed of switched cap circuits

• Integrated in ST 28nm FD-SOI CMOS

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply [V]</td>
<td>1.0</td>
<td>1.2</td>
<td>1.0</td>
<td>1.0/1.8</td>
<td>1.1</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.18</td>
<td>0.59</td>
<td>0.22*</td>
<td>0.13</td>
<td>0.065</td>
</tr>
<tr>
<td>Resolution</td>
<td>10b</td>
<td>12b</td>
<td>10b</td>
<td>13b</td>
<td>12b</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>800 MS/s</td>
<td>250 MS/s</td>
<td>2.5*/5 GS/s</td>
<td>800MS/s</td>
<td>600MS/s</td>
</tr>
<tr>
<td>SNDR@Nyq [dB]</td>
<td>52.2</td>
<td>65.7</td>
<td>52.2</td>
<td>57.2</td>
<td>60.7</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>19</td>
<td>49.7</td>
<td>150</td>
<td>76.4**</td>
<td>19.8</td>
</tr>
<tr>
<td>FOM_W [fJ/conv-step]</td>
<td>71.4</td>
<td>126.2</td>
<td>95.8</td>
<td>162.4**</td>
<td>37.2</td>
</tr>
<tr>
<td>FOM_S [dB]</td>
<td>155.4</td>
<td>159.7</td>
<td>154.2</td>
<td>154.2**</td>
<td>162.5</td>
</tr>
</tbody>
</table>

Calibration
yes no yes yes no

[Ashish Kumar et al., ESSCIRC2016]

Only single channel work in this region of the plot.
A Digital Sine-Weighted Switched-Gm mixer for Single-Clock Power-Scalable Massive Parallel Receivers in 28FDSOI

- DDFS-driven mixer-DAC is suitable for parallel RXs:
  - Only one frequency reference
  - Harmonic Rejection Mixing
  - Power consumption scales with number of channels
- Binary-weighted Switched-Gm + 2-path filter proposed:
  - Low-voltage-technologies compatible mixer-DAC
  - Power efficient
  - Tolerant to out-of-band blockers
- Original non overlapping clock generation using body bias.
- Fine linearity tuning using body bias

### Table: Performance Comparison

<table>
<thead>
<tr>
<th>Architecture</th>
<th>This work</th>
<th>F. Gatta</th>
<th>J. Wu</th>
<th>A. Maxim</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of DDFS bits</td>
<td>8</td>
<td>8</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>Frequency range [MHz]</td>
<td>100-1000</td>
<td>48-1000</td>
<td>&gt;12</td>
<td>48-1000</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>23-33</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>HRR [dB]</td>
<td>44</td>
<td>65 (w/ RF Filter)</td>
<td>-</td>
<td>60</td>
</tr>
<tr>
<td>Image Rejection [dB]</td>
<td>42</td>
<td>62</td>
<td>70</td>
<td>65</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>2-16</td>
<td>-</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>7-13</td>
<td>5-7</td>
<td>25.4 w/ digital</td>
<td>13</td>
</tr>
<tr>
<td>Isolation [dB]</td>
<td>&lt;75</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Number of channel</td>
<td>2</td>
<td>2</td>
<td>158</td>
<td>1</td>
</tr>
<tr>
<td>Power consumption [mW]</td>
<td>19 (w/ DDFS)</td>
<td>650</td>
<td>300 (only ADC)</td>
<td>450</td>
</tr>
<tr>
<td>Power/channel [mW]</td>
<td>9.5 (w/ DDFS)</td>
<td>325</td>
<td>1.9 (only ADC)</td>
<td>450</td>
</tr>
<tr>
<td>Scalable power</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Total die area [mm²]</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>1.2</td>
</tr>
<tr>
<td>IC Technology</td>
<td>28nm FDSOI</td>
<td>65nm CMOS</td>
<td>28nm CMOS</td>
<td>0.13umCMOS</td>
</tr>
</tbody>
</table>

[Image of non overlapping clock generation using body bias]

[Image of mixer circuit]

[R. Kasri et al., CICC’17]
Inverter-based amplifier in SC $\Delta \Sigma M$

- First proof-of-concept pitch-matched fully-digital subarray beamformer IC for 3D ultrasound
  - Highest per-channel SNR with ~7x area reduction

- FDSOI Technology Enabler:
  - High integration density
  - Immune to latch-up allow the use of slewing-based amplifier using minimum length cascaded inverters
  - Low $V_{th}$ devices provide area-efficient low $R_{on}$ switches

[ M-C. Chen et al., ISSCC’17]
SleepTalker - 28nm FDSOI ULV WSN Transmitter: RF-mixed signal-digital SoC

- IR-UWB BPSK and BPM RF transmitter operated at 0.55V
- IEEE 802.15.4a compliant
- 3.5 – 4.0 – 4.5GHz channels reconfiguration
- Configurable Data Rate: 0.11, 0.85, 1.7, 6.81, 27.24Mb/s
- RF SoC: digital and RF transmit path, frequency synthesizer, DC-DC (1.2V to 0.55V) and Body Bias Generator (up to +/-1.8V, for variable output voltage)

**SoC architecture innovation enabled by FDSOI:**

- Extremely low power PLL-free architecture with aggressive duty cycling, compensated by on chip adaptive FBB for Local Oscillator tuning and trimming upon the requested transmit frequency
- Digital Power Amplifier with programmable pulse shaping enabled by body biasing control, meeting FCC spectral regulation for all channels
- High speed – ultra low voltage digital implementation enabled by FBB
- Record energy efficiency improving by 16 the State of the Art (Tx: 14pJ/bit, SoC: 24pJ/bit)

[4.6 pJ/bit, 4.6 pJ/bit]

\[G. \text{ de Streel, D. Bol et al., VLSI2016 and JSSC2017}\]
Fine-Grained AVS in 28nm FDSOI Processor SoC

- **Energy-efficient FDSOI-enabled processor SoC featuring:**
  - Intensive deployment of body biasing techniques
  - Integrated voltage regulation
    - 82-89% system efficiency with adaptive clocking
  - Fully-featured processor (RISC-V Rocket Processor)
    - 41.8 DP GFLOPS/W with integrated regulators
  - Integrated power management
    - Low-overhead power estimation
    - Programmable PMU
  - Sub-μs adaptive voltage scaling (AVS)
    - Up to 40% energy savings
  - Compact implementation:
    - Core area: 1.07mm²
    - 568k Std Cells
  - Boots Linux

[B. Keller et al., ESSCIRC2016 and JSSC2017]
Conclusion
Takeaways for Analog/RF/mixed-signal body biasing

- Unprecedented very wide $V_T$ tuning range of ~250mV for FDSOI vs ~10mV for bulk

- New “tuning knob” with no parasitic effects on the signal path (control under the BOX)

- Enhanced switches performances for all type of mixed-signal circuits

- Efficient revisited tuning/trimming strategies:
  - Process/Temperature compensation
  - Circuit reconfiguration

- Flexible and energy saving SoC solutions

- Simpler circuits revisit State of the Art
FD-SOI will Enable the Ultimate Integration for Tomorrow’s Connected World

Ultra low voltage operations with high performance.

Easy and efficient analog integration (ADC/DACs, RF, LDOs, …)

FBB for dynamic power/leakage/frequency tuning

Excellent reliability and soft-error performances

Performant Ft / Fmax, Performant passive devices

Improved noise, Lower parasitic capacitances

Adapt power consumption to load

Performance and power efficiency

The Internet of Things

Network infrastructure


David Jacquet; Frédéric Hasbani; Philippe Flatresse; Robin Wilson; Franck Arnaud; Giorgio Cesana; Thierry Di Gilio; Christophe Lecocq; Tanmoy Roy; Amit Chhabra; Chiranjeev Grover; Olivier Minez; Jacky Uginet; Guy Durieu; Cyril Adobati; Davide Casalotto; Frederic Nyer; Patrick Menut; Andreia Cathelin; Indavong Vongsavady; Philippe Magarshack, “A 3 GHz Dual Core Processor ARM Cortex TM ·A9 in 28 nm UTBB FD-SOI CMOS With Ultra-Wide Voltage Range and Energy Efficiency Optimization ”, IEEE Journal of Solid-State Circuits, Year: 2014, Volume: 49, Issue:

Raphaël Guillaume, François Rivet, Andreia Cathelin, Yann Deval, Energy Efficient Distributed-Oscillators at 134 and 202GHz with Phase-Noise Optimization through Body-Bias Control in 28nm CMOS FDSOI Technology, RFIC 2017

Ashish Kumar; Chandrajit Debnath; Pratap Narayan Singh; Vivek Bhatia; Shivani Chaudhary; Vigyan Jain; Stephane Le Tual; Rakesh Malik, “A 0.065mm2 19.8mW single channel calibration-free 12b 600MS/s ADC in 28nm UTBB FDSOI using FBB”, ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Year: 2016, Pages: 165 – 168

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Robin Wilson; Edith Beigne; Philippe Flatresse; Alexandre Valentian; Fady Abouzeid; Thomas Benoist; Christian Bernard; Sebastien Bernard; Olivier Billoint; Sylvain Clerc; Bastien Giraud; Anuj Grover; Julien Le Coz; Ivan Miro Panades; Jean-Philippe Noel; Bertrand Pelloux-Prayer; Philippe Roche; Olivier Thomas; Y. Thonnart; David Turgis; Fabien Clermidy; Philippe Magarshack, « A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, embedding FMAX tracking », 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014, Pages: 452 - 453

Edith Beigné; Alexandre Valentian; Ivan Miro-Panades; Robin Wilson; Philippe Flatresse; Fady Abouzeid; Thomas Benoist; Christian Bernard; Sebastien Bernard; Olivier Billoint; Sylvain Clerc; Bastien Giraud; Anuj Grover; Julien Le Coz; Jean-Philippe Noel; Olivier Thomas; Yvain Thonnart, « A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking », IEEE Journal of Solid-State Circuits, 2015, Volume: 50, Issue: 1, Pages: 125 – 136
