Differential Complementary Millimeter wave power amplifier for 5G using 45RFSOI Process

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INTRODUCTION

• This paper is presenting the design support for a 28GHz power amplifier in the 45RFSOI technology.

• General Statement
  – 45RFSOI technology

• Design Approach
  – Transistors.
    • Size, biasing, Layout
  – Power stage
    • Structure, layout, load conditions
  – Matching structure (input/output)
    • Design, Layout, Simulations

• Conclusions
General Statement

• 45RFSOI technology has a unique capability that can be exploited for CMOS PA. It has a very good complementary set of devices (P and N) that was specifically designed for complementary high speed.

  – These characteristics are unmatched in any other technology available for RF/mmW circuits.
  – Provided designs are made specifically to use such capabilities, new opportunities can be derived for architecture of different blocks used in RF/mmW field.

• We will present here the application of the complementary technology to mmW power amplifier
• 5G will bring unique services and network capabilities, as it will entail the use of millimeter Wave bandwidth with enhanced mobile broadband, ultra reliable and low latency communications.

  – It is very likely that use of beamforming will enable higher capacity for the networks and only CMOS integration will be able to provide the miniaturized antennas feeds for steerable arrays.
General Statement

• 5G mmW power amplifier will need to function without “too much” distortion of the highly linear signal that can be a 64-QAM or even 256QAM for high Power and bandwidth efficiency.

  – The sources of non-linearity of a CMOS transistor are not strongly dependent on frequency (they are strongly dependent on power level).

  – Most of the effects can be represented by component models variations over bias variations (for example: $\Delta C_{gs}$ with $\Delta V_{gs}$).

  – Because circuits are generally tuned over frequencies to resonate the reactive elements, these variations will have a severe impact of center frequency shift and as a consequence, on EVM for the output signal.
Design Approach: Transistor design

- **Transistor Specifications**
  - The 45RFSOI has multiple sets of devices (PMOS+ NMOS) available, but we did concentrate on the highest Fmax devices for our application

- $L_{des} = 40 \text{nm (nom)}$, width = $1 \mu m \times 20$
- Double sided gate contact
- De-embedded to M1
- 1x pitch $f_T = 251 \text{GHz}$, $f_{\text{MAX}} = 313 \text{GHz}$
- 2x pitch $f_T = 296 \text{GHz}$, $f_{\text{MAX}} = 342 \text{GHz}$

- $L_{des} = 40 \text{nm (nom)}$, width = $1 \mu m \times 20$
- Double sided gate contact
- De-embedded to M1
- 1x pitch $f_T = 191 \text{GHz}$, $f_{\text{MAX}} = 256 \text{GHz}$
- 2x pitch $f_T = 245 \text{GHz}$, $f_{\text{MAX}} = 302 \text{GHz}$
Design Approach: Complementary Pair design

Transistor Specifications

NFET Size: Width=800µm Length=0.040µm

PFET Size: Width=1000µm Length=0.040µm
Design Approach:
Complementary Pair design $|V_{ds}|=0.6v$, $|V_{gs}|=0.45v$

NFET Sparameters in Red

PFET Sparameters in Blue

NFET Size: Width=800µm Length=0.040µm

PFET Size: Width=1000µm Length=0.040µm
A strong match of NFET and PFET can improve drastically the linearity of the Push-Pull stage when compared to the stage common source device AM to PM.

Graph extracted from:
A 69GHz-Power amplifier with AM-PM Distortion Cancellation in 40-nm CMOS
Kulkarni and Reynaert
IEEE Transactions on MTT Vol 64 N°7 July 2016
NFET/PFET devices Stacking

Power output target: 26dBm (400mW):

400mW translates into a max. voltage of 4.5V rms

We use two NFET and two PFET in the design of the PushPull structure. It will guarantee less than 1V DC on each device and a maximum peak voltage of 1.5V on each device.

RF model for the stacked Push Pull devices
NFET/PFET Device Layout Strategy

- we opted for a 10 fingers of 1 µm width unit cell to create a smaller connection width on the drain and source side.
- We opted for 2x Pitch for higher frequency behavior
- For voltage swing capability, we decided to use Single Gate transistors cascaded (T1, T2) and not dual gate transistor.
- We are using a structure of devices unit blocks that are interleaved in the following way for the two N-type transistor (same for P-Type)
NFET/PFET Device Layout Strategy

• Because of the current limitations in the transistors, we are using the following approach to limit the combining losses:
  
  • Metal layers M1 to M3 are stacked on the source and drain fingers
  
  • U1 metal (above M layers) to connect the fingers together with half of the metal covering the unit finger and half above the metal
Push Pull Differential One Stage Amplifier

- Differential structure provides higher symmetry for the positive and negative swing
- On-wafer measurements will allow for DPD experiments
Integrated Matching structures

• SOI technology is providing lower loss than standard substrate so integration of passive components is possible without compromise, especially at mmW frequencies

• Layout of the transformer (differential combiner) circuit:

• This structure is scalable in terms of
  – $W =$ width of the line
  – $S =$ spacing between line
  – $AP =$ Input inductor periphery

• Each EM simulation/optimization is running during the overall circuit simulation
Results from 27GHz to 29GHz

Forward Transmission, dB

freq, GHz
Results from 27GHz to 29GHz
Results from 27GHZ to 29GHz
Power PAE GAIN

[Graph showing the relationship between RF power and PAE/GAIN]
Conclusions

High frequency Complementary devices process from Global Foundries (45RFSOI) allows:

Higher level of integration for RF and mmW linear power amplifiers by

• Strong symmetry PMOS/NMOS
• Active Devices-Only amplifier design (No inductive loads).

However, new challenges are presented:

DC voltage split control between Positive and Negative side of the Push-Pull stage over load and process variations (Bias circuit has to be more complex while still microwave transparent) while keeping linearity

Incorporate Digital Pre-distortion and Vdd Control for higher linear efficiency and increased control of power dynamic range

But all of these issues can be solved with CMOS integration
Thank You

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