Design of Advanced Applications Processors in FD-SOI

MAGGIE QIU (仇雨菁)

DIRECTOR OF ENGINEERING (恩智浦微处理器事业部研发总监, 恩智浦强芯总经理)

NXP SEMICONDUCTORS

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i.MX – Applications Processor for Automotive, Industrial and Consumer
i.MX Driving Explosive Growth in Automotive and Smart Devices

Over 400M i.MX SOCs shipped to date
Over 113M vehicles enabled with i.MX since 2007

#1 in eReaders, #1 in Auto Infotainment Applications Processors

Source: IHS Technology, Q2 2015
Recent IoT Systems Powered by i.MX Processors

Benesse: Educational Tablet
OrCam: Eyeglasses for visually impaired
BMW: i series remote key
Foryou: Car Infotainment
HSAE: Car Infotainment

Home Automation & Building Control: AMX, Lennox, Honeywell, Leviton, Electrolux
Transportation: Dreamliner Inflight Entertainment, Austin B-Cycles, John Deere Tractor
Hertz Neverlost
Pioneer Nex In-Dash Navigation

SONY HAP-S1 HDD, Lenbrook Bluesound Node, Aether cone
SONY, Amazon, Kobo eReaders
POS
Medical: Masimo, Philips, Withings, etc.

8 of top 10 Automotive OEMs Infotainment Systems
6 Top Luxury Brands
Reconfigurable LCD Instrument Clusters
PPA Requirements for Different Applications
Embedded Processing – Yesterday’s Paradigm

MPU

40/28nm

High Performance, High-level OS, Graphics/Video/Display Processing

16/14/10/7nm

MCU

130/90nm

Low Power, Real-time OS, RF/NVM/Mixed Signal Integration

40/shrink
Embedded Processing – Future

- High Performance, Power Efficiency
- Mixed-Signal, Broad Scalability

- operations-led 'sustaining'
  Reuse existing foundry tooling

- Manufacturable Flash Processes

- FD-SOI Shrink
  Next-Gen Back-End Memories

- 28

- 90 / 40

- Computation & Machine Learning

Embedded Processors

FD-SOI

Manufacturable Flash Processes
FD-SOI Technology
FD-SOI Transistors vs. Bulk Transistors

Bulk Transistor

Channel Forms in Bulk Silicon

PD-SOI Transistor

Body is Partially Depleted and ‘floats’ independent from Bulk substrate

Floating Body boosts performance but introduces some peculiarities (History Effect, kink)

Tsi ~ 70nm, Tbox ~ 145nm

FD-SOI Transistor

Ultra-Thin Body (undoped)

Ultra-Thin Body is Fully Depleted

Box can optionally be ultra-thin, too

Addresses scalability issues
No History Effect
No kink effect

Tsi ~ 5-10nm (e/o process)
Tbox ~ 145nm / Tubox ~ 10-30nm

(SOIconsortium_FDSOI_QA.pdf, April 2010)
Intrinsic Advantages of FD-SOI

1. **Reliable**
   Shorter channel length, reduced variability

2. **Safer**
   Immunity to latch-up and soft errors

3. **Low Leakage**
   Leading low power capability

4. **Most Scalable Solution**
   Perfect for high performance & low power design
Wide Range of Design Options to Choose From

1. 2 VTs & 4 Gate Lengths
   - RVT and LVT available
   - Within same VT, different gate length modulates power/performance

2. Wide Range of Voltage Range
   - Nominal 1.0V
   - Overdrive 1.1V
   - Underdrive 0.9V
   - Low Voltage 0.8V and below

3. Forward Biasing & Reverse Biasing
   - RVT theoretically supports 0.3v FBB to ~2.5V RBB.
   - LVT theoretically supports 0.3v RBB to ~3.0v FBB

4. Other
   - Power gating
   - Retention
Existing Physical Implementation Flow Applies

- RTL
- Synthesis
- Timing constraints development
- Place and Route
- Timing
- STA
- IR drop analysis
- Timing Signoff STA
- Detail route
- CTS
- Timing Optimization
- Placement
- Floorplanning
- Static checks
- Physical design
- Physical design database
- Tape out (PG)
- Package co-design
- Electrical analysis
- Physical design signoff checks
- GLS
- DV / DFT
- Timing Off
- External Dependency
- Physical Design
- Place & Route
- STA
- Synthesis
There are More to Consider …

- Different VTs cannot be mixed
- Special guardring required to isolate different VTs
- FBB/RBB difficult to mix
- Special biasing generation logic required for body biasing
- More PVT corners, more complexity for physical design
Early Architecture Tradeoffs

• Overdrive, Underdrive or Nominal?
• Always-ON or Switch-OFF?
• FBB, RBB or none?
• RVT or LVT ?
• DVFS or not ?
• How to ease timing across different power domains?
Example of Power Architecture for FD-SOI Design

<table>
<thead>
<tr>
<th>Performance</th>
<th>VT</th>
<th>Voltage</th>
<th>Body Biasing</th>
<th>Power Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>LVT</td>
<td>Overdrive</td>
<td>FBB</td>
<td>Yes</td>
</tr>
<tr>
<td>Med</td>
<td>RVT+LVT</td>
<td>Nominal</td>
<td>NA</td>
<td>Yes</td>
</tr>
<tr>
<td>Low</td>
<td>RVT</td>
<td>Underdrive</td>
<td>RBB</td>
<td>Always-ON</td>
</tr>
<tr>
<td>NA</td>
<td>RVT</td>
<td>Ultra-low</td>
<td>RBB</td>
<td>Always-ON or Retention Mode</td>
</tr>
</tbody>
</table>
Physical Implementation Challenges

- Decide corner for synthesis
- Decide corner(s) to run P&R
- CTS strategy
- Guardring methodology
- Sign-off criteria
The New Normal – Scalable Embedded Processing

High Performance

Low Power

MCU

Applications Processors

i.MX 7ULP

i.MX 8X

i.MX 8

i.MX 8QM

A53
A53
A72
A72
M4
M4

4K Video

2x GPU (8 shaders)

MIPI-DSI

MIPI-DSI

MIPI-CSI

MIPI-CSI

HDMI 2.0

1GbE

1GbE

PCIe

PCIe

USB 3.0

x32 LPDDR2/3

LPDDR4/DDR4

SPIx4

MIPI-DSI

2D/3D Graphics

2x UART x4

I2C x8

MIPI-DSI

USB

x64 LPDDR4/DDR4

Public
FD-SOI - Process Technology for the Next-Gen IoT

- High Performance
- Low Power
- Faster Cycle Time
- Easy to Implement
- Optimized Cost
THANK YOU