FD-SOI Technology

Bich-Yen Nguyen
Soitec
Agenda

1. FD-SOI technology overview
2. Markets, foundries offers & ecosystems
3. FD-SOI material & roadmap
4. Summary
Challenge of Traditional Planar Bulk Transistor Scaling

- Increased standby power dissipation
- Amplified $V_{th}$ variability
  - Impact Yield
  - Limit $V_{dd}$ scaling

Source: IBM, T.C. Chen, ISSCC 2006

new transistor architectures and materials are needed
Continue Moore Law with New Materials & Device Architectures

- 2003: SiGe / Compressed Silicon (Ghani, IEDM 03)
- 2005: SiGe / High-K Gate (Tyagi, IEDM 05)
- 2007: SiGe / Strained Silicon (Mistry, IEDM 07)
- 2009: PMOS / High-K Gate (Packan, IEDM 09)
- 2011: 22nm / Fully Depleted Devices
- 2012: 20nm / Hartmann, GSA12

Key Technologies:
- Strained Silicon
- High-K / Metal Gate
- Introduction of New Materials
- Introduction of New Device Architecture
- Fully Depleted Devices
Leakage Power is still a Major Issue Despite the Use of Hi-K Dielectric

Leakage power is still tremendously growing after insertion of the High-K/MG gate stack at 28nm node as demands for more performance and functionality.

Source: IBS
New Device Architecture: Planar FDSOI or Multi-Gate Transistor

- Thin channel (Fully Depleted) with multi gates for better gate or short channel (SCE) control
- Better gate control $\Rightarrow$ better transistors scaling
FD-SOI Transistor Advantages

- Total dielectric isolation
  - Lower S/D capacitances
  - Lower S/D leakage
  - Latch-up immunity

- Ultra thin Body
  - Excellent SCE (SS, DIBL)
  - No History Effect
  - Lower SER

- No channel doping
  - Improved $V_T$ variability
  - Improved mismatch (SRAM & analog)
  - Better analog gain
  - Reduced process cost

- Ultra thin BOX option
  - Enables Extended body biasing

- Channel mobility boost
  - Scalable down to 10nm

- Conventional planar processing
  - Lower manufacturing risk
  - Equivalent bulk design

Knobs to control Perf/Power:
- Gate bias
- Back Bias

UTBB: Ultra-Thin Body and BOX
Body factor: \( n = \ldots 1.05 \ldots \) in FDSOI; \( \ldots 1.5 \ldots \) in Bulk

- Linear current: \( I_D = \frac{\mu C_{ox} W}{L} \left( V_G - V_{TH} \right) V_D - \frac{1}{2} n V_D^2 \)
- Saturation current: \( I_{D_{sat}} = \frac{1}{2n} \mu C_{ox} \frac{W}{L} \left((V_G - V_{TH})^2\right) \)
- Sub-threshold slope: \( S = \frac{n kT}{q} \ln(10) \)
- Gain (strong inversion): \( \frac{g_m}{I_D} V_A = \sqrt{\frac{2 \mu C_{ox} W L}{n I_D}} V_A \)
# FD-SOI Transistor Advantages

## UTBB FDSOI Transistor Advantages

<table>
<thead>
<tr>
<th>Advantage</th>
<th>Benefits</th>
</tr>
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</table>
| **Total dielectric isolation**                 | • Lower S/D capacitances  
• Lower S/D leakage  
• Latch-up immunity                           |
| **Ultra thin Body**                            | • Excellent SCE (SS, DIBL)  
• No History Effect  
• Lower SER                                           |
| **No channel doping**                          | • Improved $V_T$ variability  
• Improved mismatch (SRAM & analog)  
• Better analog gain  
• Reduced process cost                                 |
| **Ultra thin BOX option**                      | • Enables Extended body biasing                                          |
| **Channel mobility boost**                     | • Scalable down to 10nm                                                 |
| **Conventional planar processing**             | • Lower manufacturing risk  
• Equivalent bulk design                                 |

**Knobs to control Perf/Power:**
- Gate bias
- Back Bias

*UTBB: Ultra-Thin Body and BOX*
FD-SOI Transistor Level Benefits

- Vth and SCE defined by complex and heavily channel and halo doping techniques
- Large Vt mismatch due to random dopant fluctuation => limit Vdd scaling
- Strong sensitivity to short channel effect
- Large junction capacitance (Cj), GIDL and Diode leakage
- Limited well bias capability

BULK

FD-SOI

- Vertical transistor layout determined by FD-SOI engineered substrate and undoped channel
- Significant improved Vt mismatch due to minimize random dopant fluctuation => enable Vd scaling down to 0.4V or lower
- Excellent SCE
- Minimum Cj, GIDL & diode leakages
- Extensive back bias capability

Vertical transistor layout determined by FD-SOI engineered substrate and undoped channel
FD-SOI superior SER enables high reliability required applications

“Attractive SEU resistance due to very low charge collection volumes in FD-SOI”
Michael L. Alles Vanderbilt University, S3S conference, 2015

Mobileye using STM FD-SOI 28nm technology for their 4th gen chipset
From Assisted to Autonomous Driving

- Market leader in vision based solutions with presence in more than 27 car brands**. More than 70% market share*
- 4th generation under development exploiting full autonomous driving in cooperation with Mobileye leveraging on ST 28nm FD-SOI process

ST. P. Magarshack, Shanghai FDSOI forum, 2015
FD-SOI Transistor Advantages

Knobs to control Perf/Power:
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- Back Bias

UTBB FDSOI Transistor Advantages

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<td></td>
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</table>

UTBB: Ultra-Thin Body and BOX
FDSOI Structure by IBM - VLSI 2009

Insitu doped SiGe S/D:
⇒ Lower S/D resistance
⇒ Reduces parasitic capacitance

Lg = 25nm
Tsi = 6nm
Tinv = 1.6nm
loff = 3nmA/um
Ion-N = 570um/um
Ion-P = 550uA/um
Vdd = 0.9v
## IBM: 28LP Bulk vs. FDSOI 20LP

<table>
<thead>
<tr>
<th>Parameter</th>
<th>28LP Bulk IBM et al. (*)</th>
<th>ETSOI IBM et al. (**)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg</td>
<td>30nm</td>
<td>22nm</td>
</tr>
<tr>
<td>VDD</td>
<td>1V</td>
<td>1V</td>
</tr>
<tr>
<td>Ion @ Ioff=300pA/um</td>
<td>660µA/µm</td>
<td>380µA/µm</td>
</tr>
<tr>
<td></td>
<td>Ion @ Ioff = 1nA/um</td>
<td>740µA/µm</td>
</tr>
<tr>
<td>DIBL</td>
<td>120mV/V</td>
<td>130mV/V</td>
</tr>
<tr>
<td>AVt</td>
<td>2mV.µm</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>1.1V</td>
<td></td>
</tr>
</tbody>
</table>

(*): IBM Alliance 28LP technology as reported at IEDM’09, F Arnaud et al.
(**): ETSOI technology for 22/20LP from IBM Research, as reported at FDSOI workshop dec 2010.
### FD-SOI Transistor Advantages

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| No channel doping                 | • Improved $V_T$ variability  
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| Ultra thin BOX option             | • Enables Extended body biasing                                        |
| Channel mobility boost            | • Scalable down to 10nm                                                 |
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• Equivalent bulk design           |

**UTBB: Ultra-Thin Body and BOX**

Knobs to control Perf/Power:
- Gate bias
- Back Bias

Courtesy of STM
SOI value: part of device integrated by substrate engineering

- Optimized SOI wafers provide excellent silicon geometry control
  - To make the best of FD technology

**Soitec FD-2D wafer**

- Ultra-Thin Top Silicon Layer
- Ultra-Thin Buried Oxide
- Base Silicon

**FD-SOI transistor**

- Critical dimension: Top Si thickness
- Critical dimension: channel thickness

Enables:
FDSOI Uniformity: Lowest VT variability

Record and reproducible low $A_{VT}$ of 1.25mV.$\mu$m @ Lg=25nm (32/28nm GR)

±2.6A, 2mm EE- 721 pts F5X inspection

Gate Length (nm)

Silicon Thickness vs. Vt

Vt sensitivity is 25mV/nm -> need > Tsi +/- 5nm

Cheng et. Al. IBM IEDM 2009

B. Doris et al., FD-Workshop at SFO, 2012
50-60% Vt variation improvement by using undoped channel retains with technology scaling
Single Port 4Mb SRAM: No Back Bias

✓ Improved memory minimum voltage

28nm LP Bulk vs 28nm FDSOI from STMicroelectronics (gate-first HKMG Technology)
Planar UTBB FD-SOI: Some Facts!
Reduced Devices Variability
FDSOI for RF & Analog Beyond 28nm Bulk

- **FDSOI key analog differentiations**
  - Higher Analog Performance vs Bulk
  - Lower variability than bulk
  - Lower Capacitance enabling higher frequency
  - Lower Phase noise
  - Remaining planar

- **On the fly Vt tuning**
  - New circuit topology enabler: double gate transistor
  - Analog: VT, Fmax, Gm, Ioff, ....

- **Ideal for next generations transceivers and SoC**

![FDSOI vs Bulk CMOS comparison](image)

- Gain @ Lmin
- Gain @ Id
- Variability (Undoped Channel)
- Fmax > 300Ghz
FD-SOI Transistor Advantages

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UTBB: Ultra-Thin Body and BOX
Electrostatic Scaling Rule of FDSOI down to Lg~10nm

- Electrostatic control improved by thinning $T_{\text{box}}$ and $T_{\text{Si}}$
- Superior short-channel control maintained with scaling
- Scalability possible down to Lg~10nm, thanks to UTBB FDSOI
Multi-VT Solution for FD-SOI with Dual Metal Gate/Ground Plane

O. Weber et al., IEDM'10

- Multi Vt requirement for SoC can be achieved for FDSOI device using dual WF metal-gate and ground-plane approach without back-bias
Multi-VT Modulation for FDSOI with Back Bias

VT tuning with BOX = 10nm and VBB, GP

N and PMOS: VT modulation of ≤200mV for 10nm BOX

No degradation of Ion-Ioff trade-off with back-bias up to +/-2V
Body-Bias enabling wider dynamic operating range
NXP example (BB level 0)

FD-SOI  Enabling Wide Dynamic Operating Range

- Outstanding Power-Perf demonstrated
  - Active mode @ 300MHz < 10mW
  - Deep-sleep with SRAM retained: < 2.5μW
  - Extremely low-leakage SRAM: ~ 0.5pA/bit

- Forward Body Bias (FBB)  Expanded performance
- Reverse Body Bias (RBB) Lower leakage floor
- Dynamic biasing tunability

Source: NXP presentation at SOI Consortium, Santa Clara, April 2017
FD-SOI with Back Bias enables 0.4v Operation for IoT

FDSOI 0.08um2 SRAM (80nm CPP)

- SRAM remains functional down to $V_{DD}=0.4V$
- Clear SNM modulation from back bias
- Both Stability and Vt variation improved with RBB
- Lower Vdd for logic operation with software controlled Back-bias enables SoC Product with tremendous power saving (>70%)

Q. Liu, et. al. VLSI Symposium 2011
R. Tsuchiya, et. al. IEDM 2007
22nm FDX Platform Features: ULL, ULP & RF

22FDX® Excellent Low Leakage and Low Voltage SRAM for IoT

<1 pA/cell retention current and 0.30V retention voltage with 0.110μm² bitcell @ 32Mbit
22nm FDX Platform Features: ULL, ULP & RF

What makes 22FDX® the best CMOS mmWave technology with similar or better performance to SiGe radios?

- Highest FTC/Fmax
- Highest mmWave self gain
- Lowest mmWave noise
- "mmWave FET stacking" for PA and switch integration
FD-SOI is Cooler than Bulk Technology

Cooler Smartphone can be used for longer time
Running applications simultaneously on both L8540 & L8580 platforms configured with same settings (max 1.85GHz). Monitoring temperature and power consumption for the digital part
### FD-SOI Transistor Advantages

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**Knobs to control Perf/Power:**
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**UTBB: Ultra-Thin Body and BOX**
FDSOI Scalability: Boosters Roadmap

- 28nm FDSOI
  - +30% Speed
  - +30% power (@ same speed)

- 22/14nm FDSOI
  - -30% power (@ same speed)
  - +20% Speed
  - -25% power (@ same speed)

- 12/10nm FDSOI

- In situ doped RSD
- Vt and µboost
- SiGe Channel for PFET
- µboost
- Racces
- Boosted back bias
- SSOI
- 2nd gen RSD + cSiGe
- 15nm Box

FD-SOI technology
FDSOI Performance Booster: local Ge Condensation for PMOS
Strain SiGeOI by Ge Condensation of SOI

Source: S. Nakaharai, Appl. Phys. Lett. 83, 3516 (2003);

- Local Ge condensation with various Ge content/strain level has been used to boost hole mobility or P-type MOSFET performance

\[
\mu_{\text{eff}} = \frac{\mu_{\text{eff}} (V_G - V_T)}{\mu_{\text{eff}} + 2V_{\text{sat}} L/(V_G - V_T)}
\]

\[W C_{\text{ox}} V_{\text{sat}}\]
Performance of PMOS using cSiGe channel formed by Local Ge Condensation

- NMOS does not degrade with local Ge condensation process
- Compressive SiGe channel PMOS improved by 35% over unstrained Si FDSOI

Source: IBM, Cheng et. al, IEDM-2012
ARM says 22nm FD-SOI with proper BB optimization outperforms FinFET at pure performance standpoint.

Selective back-gate biasing is developed by ARM.

Using proper BB on 22nm FD-SOI can achieve higher performance/power tradeoff as those of 14 FinFET technology for ARM HP CPU (Cortex-A72).

Source: ARM, SOI Consortium San Jose 2016
FDSOI Performance Booster: Tension Strain Si Channel for NMOS
Strained Si on Insulator (sSOI) for boosting NMOS Performance

- Demonstrated 75% long channel mobility and 27% short channel performance increase.
- In addition, 20% \( I_{ON} \) increase is achieved by a new ISPD Si epi.

Source: IBM, Khakifirooz et. al, VLSI-2012
# 10nm FD-SOI and DC Performance Comparison

## A Comparison of Devices in this work with State-of-Art FinFET and FD-SOIJ Devices

<table>
<thead>
<tr>
<th></th>
<th>*Auth et al VLSI 12</th>
<th>*Jan et al IEDM 12</th>
<th>Wu et al IEDM 13</th>
<th>Weber et al VLSI 14</th>
<th>This work</th>
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<tbody>
<tr>
<td>$V_{dd}$ (V)</td>
<td>0.8</td>
<td>0.75</td>
<td>0.75</td>
<td>0.8</td>
<td>0.75</td>
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<tr>
<td>N/P DIBL (mV/V)</td>
<td>46/50</td>
<td>30/35</td>
<td>52/42</td>
<td>56/51</td>
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</tr>
<tr>
<td>N/P SS (mV/dec)</td>
<td>69/72</td>
<td>71/72</td>
<td>73/71</td>
<td>78/78</td>
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<tr>
<td>$I_{off}$ (nA/μm)</td>
<td>100/1</td>
<td>100/1</td>
<td>100/1</td>
<td>100/1</td>
<td></td>
</tr>
<tr>
<td>$L_C$ (nm)</td>
<td>30/34</td>
<td>30/34</td>
<td>30/34</td>
<td>20/34</td>
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<table>
<thead>
<tr>
<th></th>
<th>NFET $I_{on}$ (mA/μm)</th>
<th>NFET $I_{eff}$ (mA/μm)</th>
<th>PFET $I_{on}$ (mA/μm)</th>
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<tr>
<td></td>
<td>1.26/0.88</td>
<td>0.65/0.42</td>
<td>1.1/0.78</td>
<td>0.56/0.38</td>
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<td>1.08/0.71</td>
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<td>1.01/0.75</td>
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<td></td>
<td></td>
<td></td>
<td>0.5/0.26</td>
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</table>

* Drive/effective current is normalized to footprint, which is 20~30% higher than normalized to effective channel width.

Source: Q. Liu et. al, IEDM 2014
### FD-SOI Transistor Advantages

#### UTBB FDOI Transistor Advantages

| Total dielectric isolation | • Lower S/D capacitances  
|                          | • Lower S/D leakage  
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**Knobs to control Perf/Power:**
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*UTBB: Ultra-Thin Body and BOX*
Simplicity of the FDSOI Integration

1- Isolation:
   - Shallow Trench Isolation
   - Define the bulk/SOI area (hybrid option)
   - Ground plane implant

2- Gate Stack:
   - Sac Ox and High-K deposition
   - Metal gate & poly Si deposition
   - Gate stack patterning, etch, HfO2 removal

3- Source/Drain formation
   - Selective epitaxy growth (insitu doped or undoped with extension & S/D implant)
   - Salicidation

4- MOL and BEOL
   - ILD/Via/Metal Interconnect Backend
28nm FDSOI Process Migration

36 masks for
- Dual Vt core oxide
- 1.8V I/O oxide
- Full active/passives offer
- Full bitcells offer
- Deep Nwell
- 7 metal levels BEOL stack
- RDL
Global Foundries 22nm FD-SOI Process Flow

- Base process leverages ~75% existing modules in 28nm production flow.
- Logic/SRAM die scaling: 0.72x/0.83x.

38 Masks and 8 metal Levels
65/45/28nm FDSOI
- UTBB substrate
- Elevated Si EPI S/D

22/14nm FDSOI
- UTBB substrate
- SiGe Channel for PMOS
- In situ doped SiGe and SiC EPI for S/D

10nm FDSOI
- sSOI substrate
- SiGe Channel for PMOS
- In situ doped SiGe & Si(C) EPI for S/D
FD-SOI: FinFET performance at lower manufacturing cost

**FDX™** – The simple solution for advanced node performance
Next node performance with 40 percent fewer masks

**Performance (a.u.)**

- 22FDX
- 16/14nm FinFET
- 12FDX
- 10nm FinFET

**Masks (a.u.)**

- 22FDX
- 16/14nm FinFET
- 12FDX
- 10nm FinFET

- FinFET digital performance & power
- Superior Analog/RF to FinFET
- Performance on demand w/ Body-bias
- 40% fewer masks
- Lower mask cost
- Reduced cycle time

Source: Based on GF internal assessments

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FD-SOI brings many differentiation in Mobile, IoT, 5G & Automotive markets

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<th>Mobility</th>
<th>IoT</th>
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<tbody>
<tr>
<td><strong>Best Power/Perf/Cost solution for</strong></td>
<td><strong>Perfect fit for</strong> wireless &amp; ULP / ULL IoT clients in need of:</td>
</tr>
<tr>
<td>› Low-mid tier <strong>Baseband + AP</strong></td>
<td>› On-demand processing performance</td>
</tr>
<tr>
<td>› 4G transceiver integration</td>
<td>› Integrated RF</td>
</tr>
<tr>
<td>› 5G mmWave design</td>
<td>› Embedded memory</td>
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<tr>
<th>5G &amp; Radars</th>
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</tr>
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<tbody>
<tr>
<td><strong>Ideal technology for</strong></td>
<td><strong>Unique advantages in low power/ high reliability (SER)</strong></td>
</tr>
<tr>
<td>› <strong>5G mmWave</strong> low power single chip solution with integrated PA</td>
<td>› <strong>ADAS</strong> (&lt;5W) for autonomous driving</td>
</tr>
<tr>
<td>› &lt;6GHz applications w/ 35-50% die shrink (LTE, Wifi,...)</td>
<td>› <strong>Radar</strong> - Mid to long range single chip</td>
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<td></td>
<td>› <strong>Infotainment</strong></td>
</tr>
<tr>
<td></td>
<td>› <strong>MCU</strong> for Body Electronics</td>
</tr>
</tbody>
</table>

FD-SOI global wafers estimate: 2021 (est.): 1-3M wafers/y.

Source: Soitec estimates
The FD-SOI Revolution has started in Consumer & Automobile

**Consumer**: a game changer technology for better battery life

- FD-SOI technology unlocks battery-powered device potential
  
  - FD-SOI based Sony GPS to cut standard GPS power consumption by 5 to 10x
  - Now, more than a day autonomy with GPS ON

- i.MX based reference platform developed by NXP for Amazon’s Alexa
- FD-SOI is a key enabler of the i.MX reference platform for always-on applications

**Automotive**: best power efficiency allowing simpler integration and enhanced reliability

- FD-SOI - reference technology for ADAS level 3 applications
- Next generation e-Cockpit solution with full management of car infotainment
  
  - Level 3 autonomous driving
  - 2.5Tops @ only 3W
  
  - Advanced features - object recognition through neural network

Now, more than a day autonomy with GPS ON
FD-SOI: Strong traction from foundries

**28FDS - Production status**

- Technology qualified in 1Q15, and is ready for mass production
- The first commercial production started in 1Q2016
- 12 product T/Os completed in 2015, >10 planned in 2016
  - **Current**: Network, set-top box, security, game, connectivity, AP for consumer, automotive ADAS and CIS
  - **Next**: Wider automotive application, IoT, wearables, MCU, programmable logic
- Technology offering updates:
  - **Single platform** technology offering (2Vts, body and gate biasing, overdrive)
  - **RF add-on**: Production PDK by 3Q16
  - eNVM add-on: mass production targeted from 2018

---

**22FDX™ Platform Extensions**

- **22FDX base platform**
  - Low-power
  - Memories
    - HD, HC, LV, ULV, TP
  - Libraries
    - 8THQ/9THQ/10THP
  - Devices
    - 4 Core Vts (FBB & RBB)
    - 2IO Vts @ 1.2/1.5/1.8v
    - Passives
  - Body-bias enabled reference flow

- **Base platform PDK & IP**

- **Application-optimized extensions**
  - -rfa adds RF enablement, BEOL passives, and IP for BLE, WiFi, ZigBee
  - -ull adds devices, libraries, and memory compilers to achieve 1pA/um leakage
  - -ulp adds logic libraries and memory compiler optimized for 0.4v logic operation
  - -mram adds efficient NVM and low-power cache replacement for IoT
  - -auto adds grade 1 for under-the-hood automotive / industrial
28nm FD-SOI cheaper cost per gate & design cost

Why 28nm?

- 28nm node is cost optimal node and 28FDS provide best in class power/performance
- 28FDS is the most suitable technology for the applications of IoT era

[Diagram showing cost per gate and design cost by process generation, with a sweet spot highlighted for 28nm.]
FD-SOI – A mainstream solution with many choices

Performance & density at any cost - for Servers, networking & High-end Mobile

FinFET 7nm
FinFET 10 nm
FinFET 16/14nm
HK, PolySi 28nm
Bulk 90/65/45 nm

28nm – ‘Last Simple Node?’

40nm to 28nm will be significant % of worldwide capacity in 2020

R. Martino - Shanghai FD SOI Forum – Sept 2015
FD-SOI – A mainstream solution with many choices

- Cost-effective & performance for Low-power applications
- Performance & density at any cost - for Servers, networking & High-end Mobile

- FinFET 7nm
- FinFET 10 nm
- FinFET 16/14nm
- HK, PolySi 28nm
- Bulk 90/65/45 nm
- FD-SOI 12 nm
- FD-SOI 18 nm
- FD-SOI 22 nm
- FD-SOI 28 nm
- FD-SOI 65 nm
- eMRAM

FD-SOI technology
FD-SOI: ecosystem getting stronger

A rapidly growing FD-SOI ecosystem

<table>
<thead>
<tr>
<th>Research Technology &amp; IP</th>
<th>Substrates</th>
<th>Foundries &amp; IDM</th>
<th>Fabless &amp; OEMs</th>
<th>Consumer Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soitec</td>
<td>Soitec</td>
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<td>Sony</td>
<td>NXP</td>
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<td>Renesas</td>
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<td>GlobalFoundries</td>
<td>GlobalFoundries</td>
<td>GlobalFoundries</td>
<td>MobileEye</td>
<td>MobileEye</td>
</tr>
</tbody>
</table>

- **GLOBALFOUNDRIES**
  - Extension of current 28 nm FD-SOI platform by incorporating RF and embedded MRAM
  - 18 nm FD-SOI process technology targeted for risk production in 2019
  - Focus on 12 FD-SOI development

- **Samsung**
  - Increasing 22 FD-SOI capacity: +40% est. in Germany by 2020
  - New 300 mm fab. in China with expected volume production in 2019

- **CEA - LETI**
  - Presented path to 10nm FD-SOI

- **IP & EDA Vendors**
  - Active position in promoting FD-SOI

Increasing 22 FD-SOI capacity: +40% est. in Germany by 2020
New 300 mm fab. in China with expected volume production in 2019

Focus on 12 FD-SOI development
Agenda

1. FD-SOI technology overview
2. Markets, foundries offers & ecosystems
3. FD-SOI material & roadmap
4. Summary
FD-SOI Substrate Maturity

- Long collaborative history on FD-SOI
  - Smart Cut & device experts 2005
  - Research Institute 2005
  - Donor substrate 2005
  - Advanced R&D 2008
  - Industrialisation 2010
  - 28FD foundry offer 2014
  - 22FD foundry offer 2015

- FD-SOI substrate reached production maturity since 2013

- Proven manufacturing capability on more than 70000 wafers
  - +/- 5Å top silicon uniformity specification met with CpK>1: all wafers, all points
  - Differential Reflective Metrology defined to predict / protect variability on device
  - Defectivity in line with foundry requirements
  - >95% device wafer yield demonstrated at foundry

Top silicon thickness
Full wafer thickness deviation (Å)
(41 points per wafer, ~15k wafers)
Thickness control

>70,000 Wafers @ ± 1 Atomic Layer!

Silicon thickness uniformity is guaranteed to within just a few atomic layers:

±5Å

±1.4cm

Soitec FD-SOI wafer

SOITEC Confidential

FD-SOI technology
Standard Smart-Cut™ process flow and FD-SOI specifics enabling ultra thin SOI film and BOX

High quality top wafer for thin SOI film compatibility

1. Initial silicon
2. Oxidation
3. Implantation
4. Cleaning and bonding
5. Splitting
6. Finishing
7. Donor wafer becomes new wafer A

Adapted to thin BOX
Adapted to thin SOI film
Adapted to thin BOX
Adapted to thin BOX
Efficient collaboration with equipment makers
Example of FD-SOI roughness management

Enhanced smoothing with Kokusai batch anneal technology

Unique chip scale thickness measurement developed with HSEB

Tool customized with new deposit management for SOI manufacturing

New tool redesign ongoing for enhanced flow management to achieve ultimate FD-SOI roughness & uniformity

Collaboration on Differential Reflective Metrology development

Full map thickness measurement – a critical parameter for FD-SOI
## A multi-nodes FD-SOI Product Roadmap

<table>
<thead>
<tr>
<th>Target node</th>
<th>65FD</th>
<th>28FD</th>
<th>22FD</th>
<th>12FD</th>
<th>Beyond 12FD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Box thick.</td>
<td>15nm</td>
<td>25nm</td>
<td>20nm</td>
<td>15 – 20nm</td>
<td>≤ 20nm</td>
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<tr>
<td>Top Si unif</td>
<td>± 1.0 nm</td>
<td>± 0.5 nm</td>
<td>± 0.5 nm</td>
<td>± 0.4 nm</td>
<td>tbd</td>
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<tr>
<td>Top Si thick.</td>
<td>30 nm</td>
<td>12 nm</td>
<td>12 nm</td>
<td>12 nm</td>
<td>Pending device</td>
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<tr>
<td>Top Si Mob.</td>
<td>Si unstrained</td>
<td>Si unstrained</td>
<td>Si unstrained</td>
<td>Si unstrained</td>
<td>Si / SiGe Strained / relaxed</td>
</tr>
</tbody>
</table>

*FD-SOI technology*
SOITEC FD-SOI wafer capacity

UP TO 1.5M WAFERS/YEAR CAPACITY WITHIN EXISTING FACTORY

Detailed Capex and Operational plans are defined for Bernin 2 (up to 500kw) and Singapore (up to 1Mw)
  * Will be triggered in coordination with foundries demand

Phase 2: Singapore fab will get full qualification at customer level in first half 2019

Phase 3 (additional >1,5Mw) is in planning stage – different options (locations, partners) are being considered
  * estimated time to qualified fab: 24 months
  * timing will be coordinated with foundries

10/10/2017  •  60  •  SOITEC Confidential  •  FD-SOI technology
Summary

- FD-SOI enables far better scalability and transistor characteristics than planar bulk
  - higher performance
  - lower power
  - better reliability
  - wider operating range through its back-bias capability

- FD-SOI is a simpler and cost-efficient process/design than other fully depleted approaches

- FD-SOI allows very strong differentiation in low power & 5G markets

- FD-SOI roadmap down to 12nm is already defined by foundry

- The value of FD-SOI is now recognized by fabless and is about to be introduced in high volume consumer products

- FD-SOI is enabled by SOITEC engineered substrates

- SOITEC has the capacity to support multi-million wafers/year supply chain

- FD-SOI ecosystem is getting ready
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