

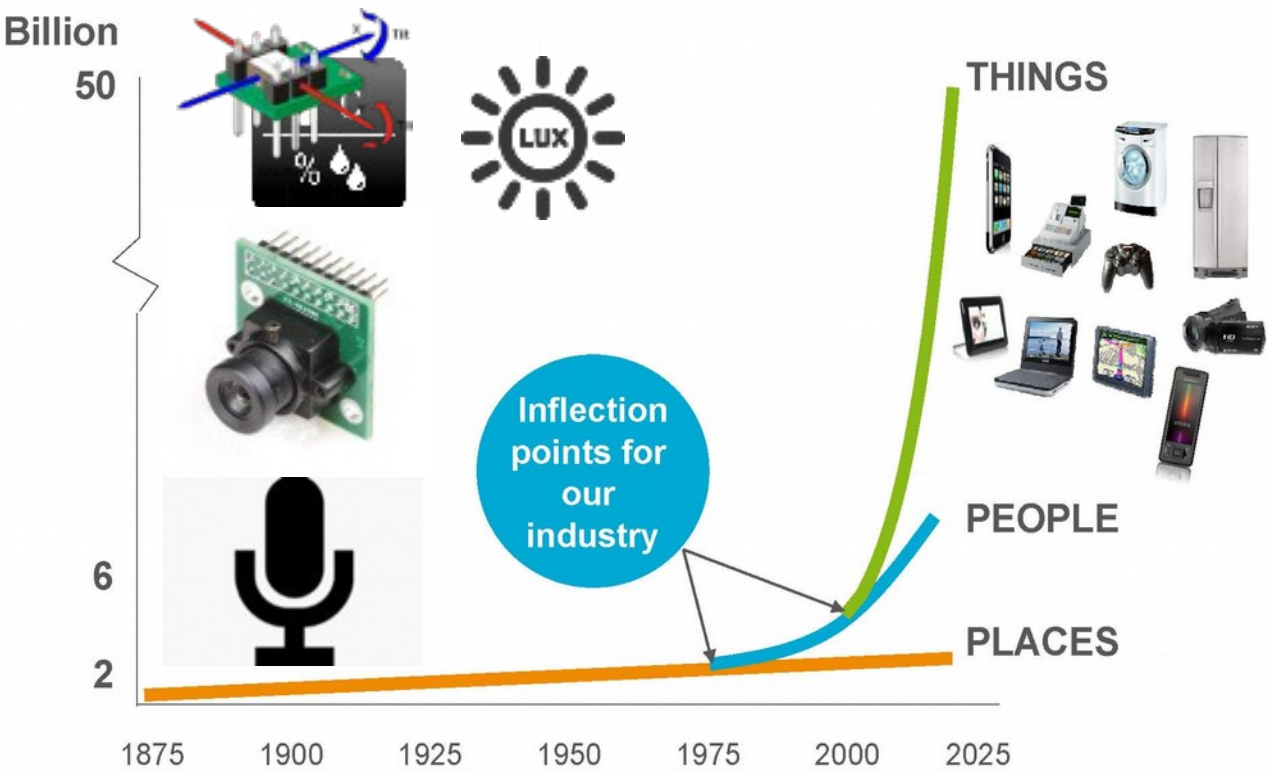
GAP8 IOT Application Processor

A PULP/RISCV BASED PLATFORM FOR NEAR-SENSOR ANALYTICS

Eric Flamand. CoFounder & CTO
Greenwaves Technologies

ANYTHING THAT BENEFITS FROM NETWORK CONNECTION WILL BE CONNECTED

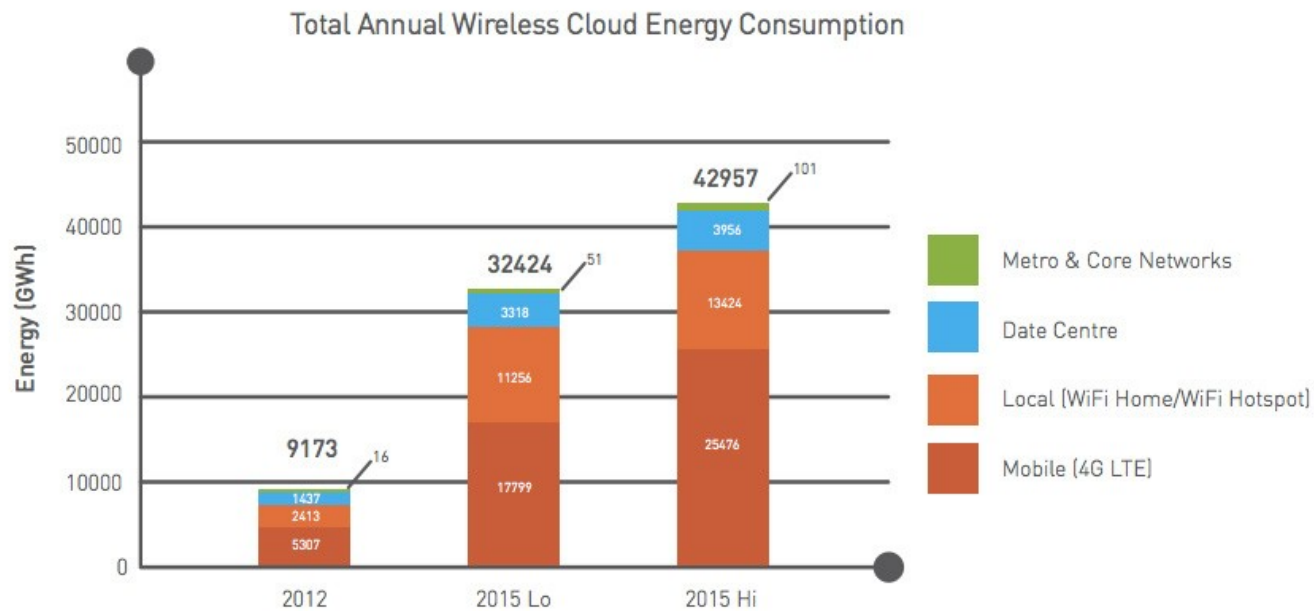
?



Source: Ericsson

Cost of transporting these data over the air ?

Serial short reach link: best results around 0.5 pJ/bit
LTE: between 300 and 600 uJ/bit



Even assuming distributed computing is marginally more efficient than centralized we win big if data volume to be exchanged over the air is srinked by several order of magnitude moving from quantitative data to qualitative data!

So in practice

If we want data reach sensors



Move from (raw) data to meta data (abstract/pertinent)
Perform this transformation close to sensor
While fitting in a tight power and cost budget
And being seamlessly integrated to the Internet over the air

Three main sources of intensive data

- **Image:** *Raw input in the order of 100KB/s for a small sensor*

- Scene classification
- Posture analysis
- Identification

Output is a single index

- **Voice/Sound:** *Raw input in the order of 10KB/s per mic*

- Recognition
- Identification
- Signature analysis

Output is a single index

- **Vibrations:** *Raw input in the order of 10KB/s*

- Preventive maintenance
- Monitoring

Output is a single index or an alarm

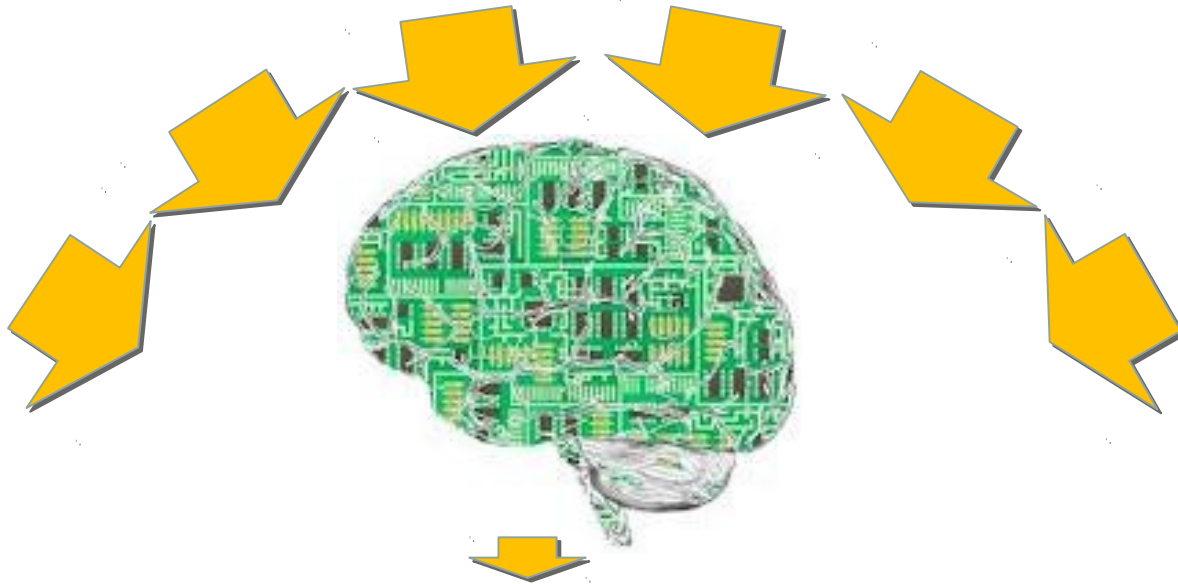
Bandwidth is reduced by several order of magnitude



Once properly processed, common denominator is: extremely compact output (single index, alarm, ...)

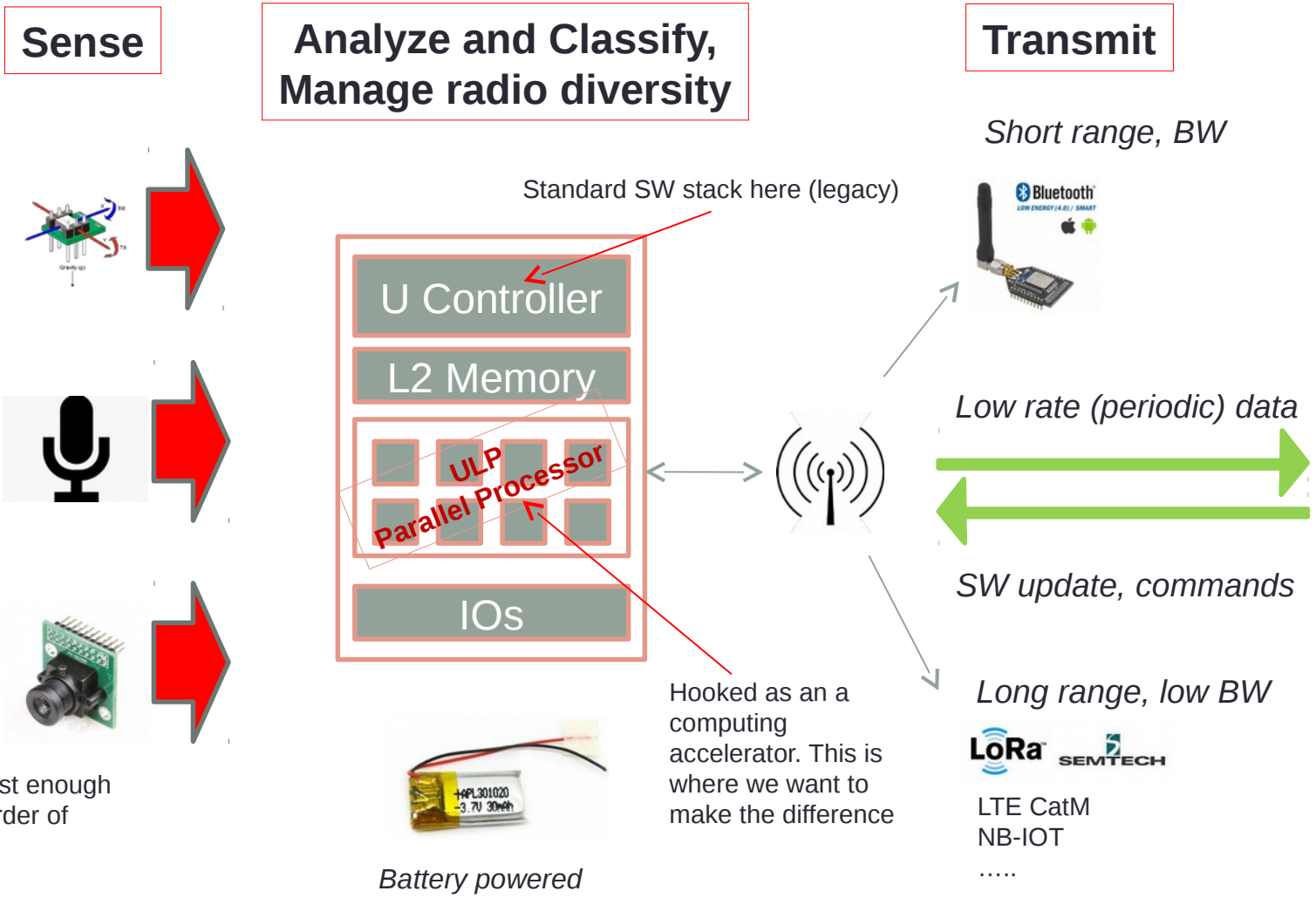
What we want to achieve

*Giga/Mega Bytes per second of **incoming** raw data from sensors*



*Few (Kilo) Bytes per second of **outgoing**, heavily processed data @ minimum Joule per operation*

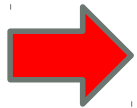
System level view



Resolution just enough for the job, order of QVGA/VGA

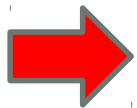
General pattern for content understanding

- Extract descriptors from raw data
 - 2D: Corners, blobs, HOG, DOG, ...
 - 1D: LPC coefficients, Cepstral coeffs, ...



Usually highly parallel

- Use descriptors to classify data among representative families
 - Machine learning (CNN, SVM, Boost), Bayesian,



Also highly parallel

Performances

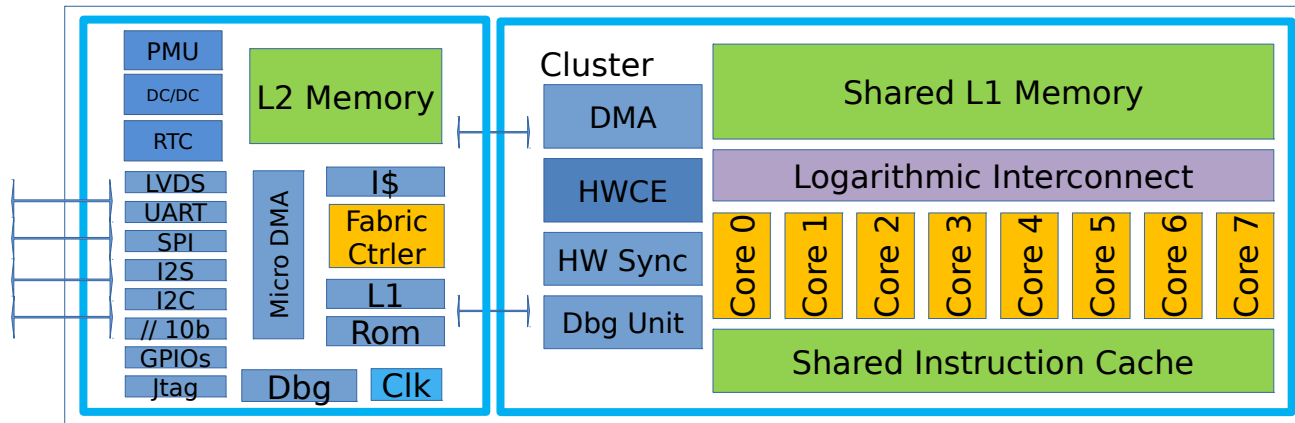
- up to 12GOPS
- up to 0.4GOPS @ 1mW,
- up to 40MOPS @ 300uW
- 3 uWatt stand-by power consumption

Architecture efficiency

- Extended Risc-V ISA
- Low contention shared memory 8 +1 core clustered architecture
- Tight synchronization
- CNN based pattern matching engine (HWCE)

HW features

- Smart IOs
- Voltage regulator/DVFS
- RTC
- Secured execution



Low cost processor

- 55nm LP
- 0.5MB L2
- aQFN 84

Leveraging open source projects

- Risc-V (Berkeley)
- PULP (ETHZ, UniBo)

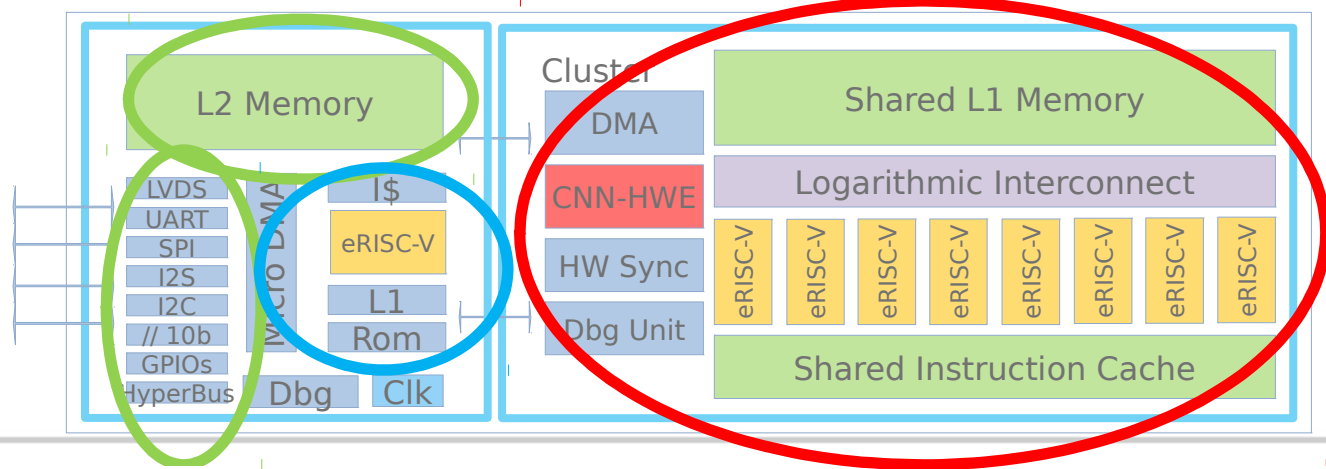
Application affinity

- Dominant signal processing part
- Limited memory requirement
- Limited SW legacy

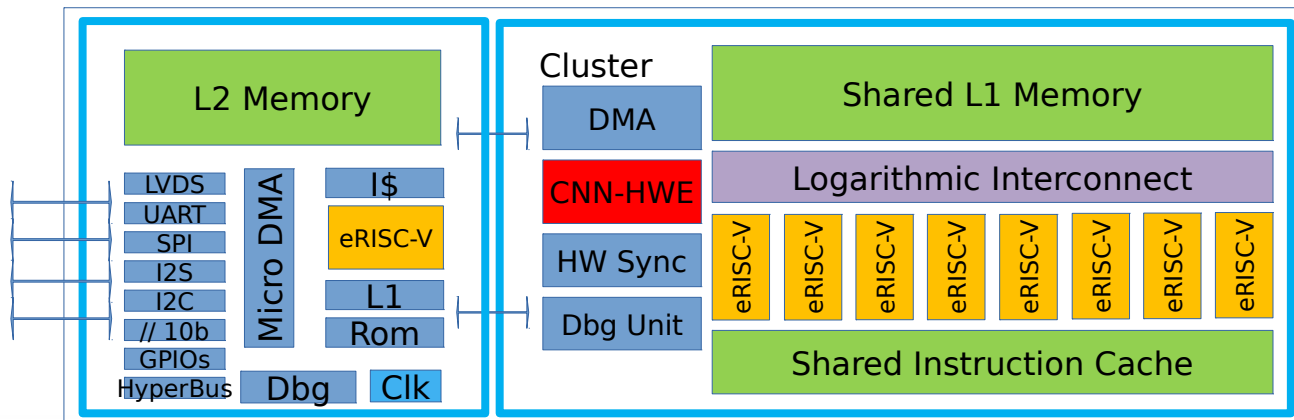
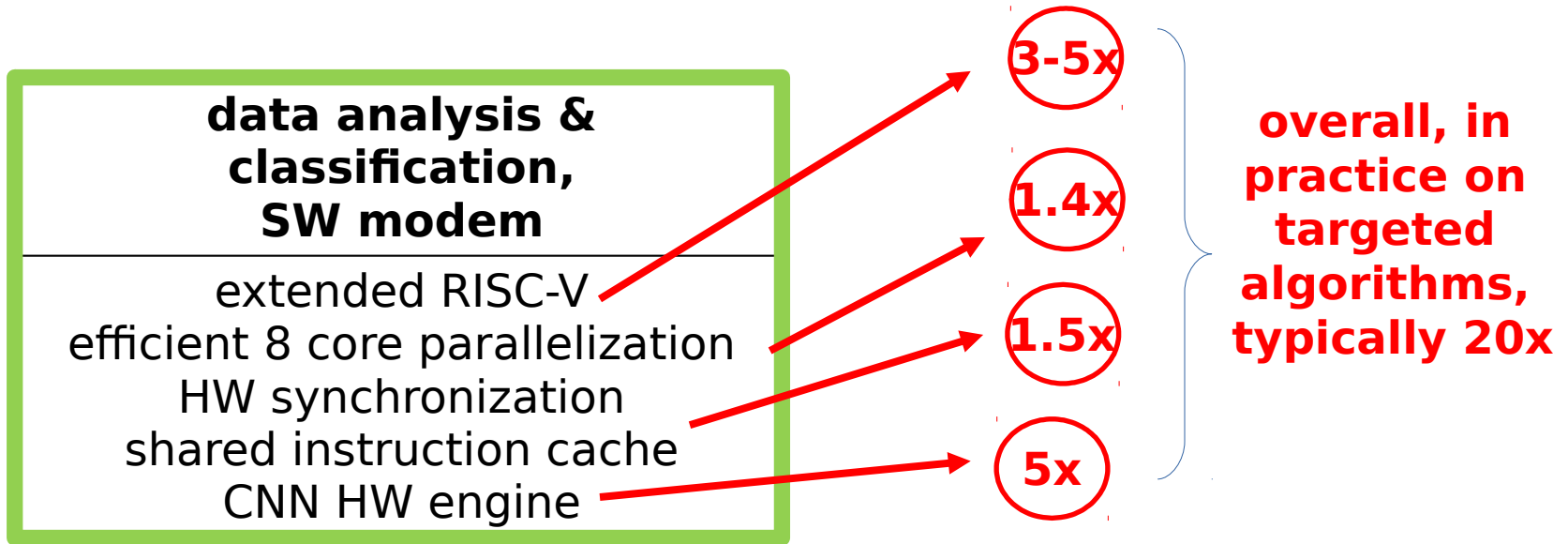
GAP8 has a unique energy efficiency across a very large range of computing power

GAP8 Hierarchical Architecture

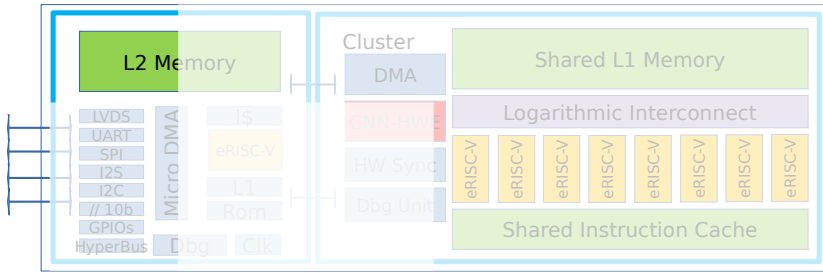
monitoring	event qualification, protocol stack, system control	data analysis & classification, SW modem
Smart I/Os voltage regulator & RTC SRAM in retentive mode	extended RISC-V	extended RISC-V efficient 8 core parallelization HW synchronization shared instruction cache CNN HW engine
quasi stand-by	low computing power	high computing power
uWs	mWs	10 to 20 mWs
primary energy consumption		primary energy consumption



GAP8 architectural energy efficiency gains



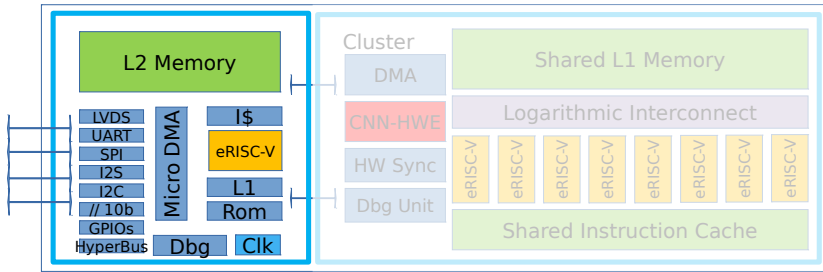
GAP8 Advanced Power Management



uW range

MCU sleep mode

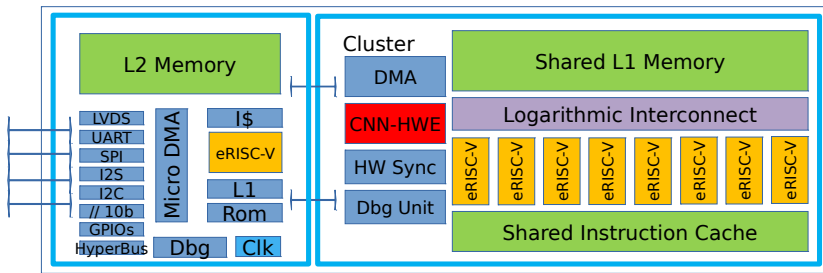
- ✓ Embedded DC/DC, low current
- ✓ Real Time Clock 32KHz only
- ✓ L2 Memory partially retentive



1 mW range

MCU active mode

- ✓ Embedded DC/DC, high current
- ✓ Voltage can dynamically change
- ✓ One clock gen active, frequency can dynamically change
- ✓ Systematic clock gating



10-20 mW range

MCU + Parallel processor active mode

- ✓ Embedded DC/DC, high current
- ✓ Voltage can dynamically change
- ✓ Two clock gen active, frequencies can dynamically change
- ✓ Systematic Clock Gating

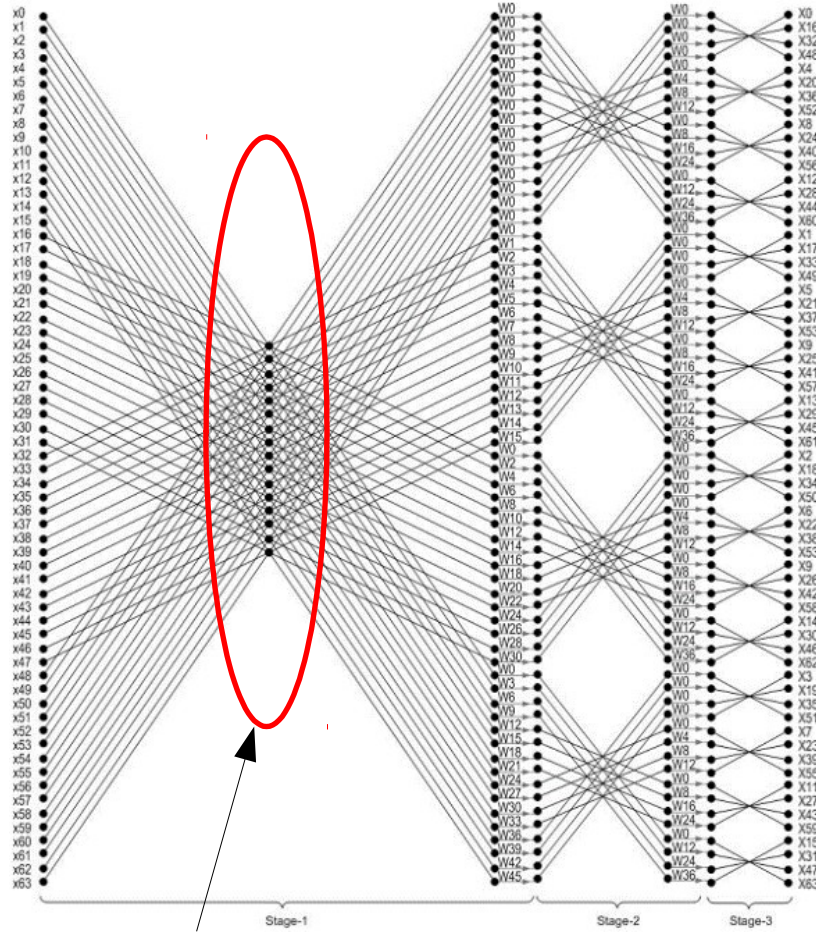
Ultra fast switching time from one mode to another
 Ultra fast voltage and frequency change time



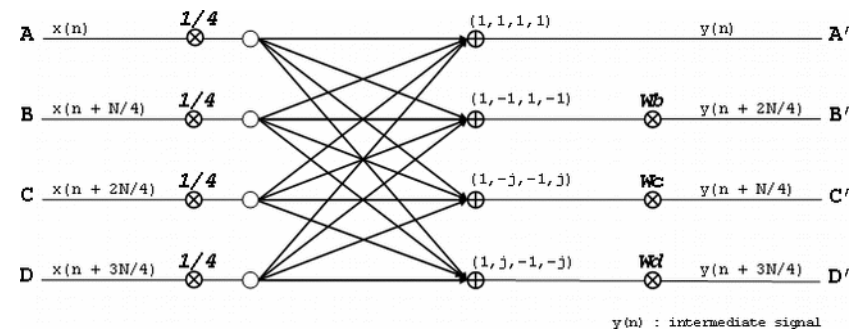
Highly optimized system level power consumption

Qualitative data from real life applications

The work horse for radio, sound and vibration: FFT



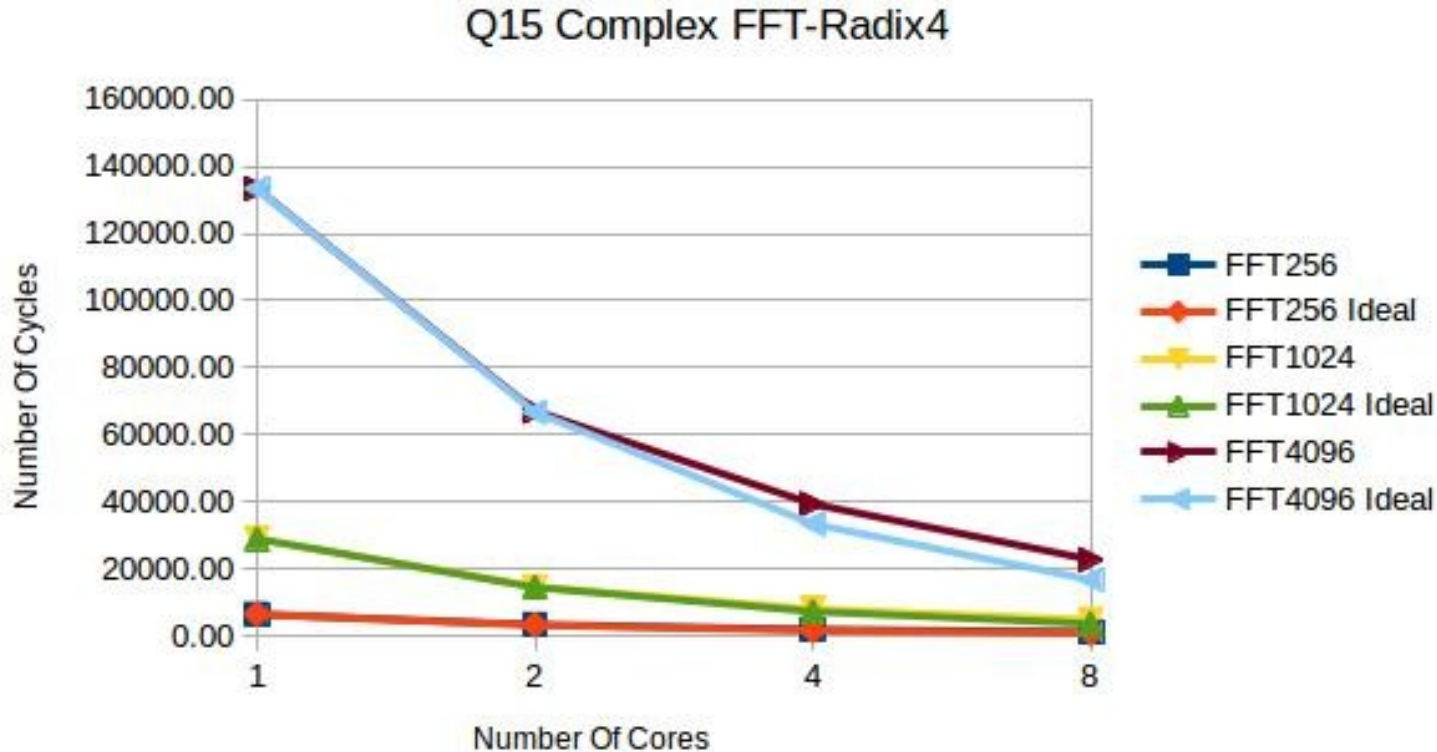
Radix4 Butterfly



- Key operations for performance
- Complex Multiplications
- Complex Rotations
- Post modified accesses
- Vectorial operations

All these butterflies are evaluated in parallel

The work horse for radio, sound and vibration: FFT



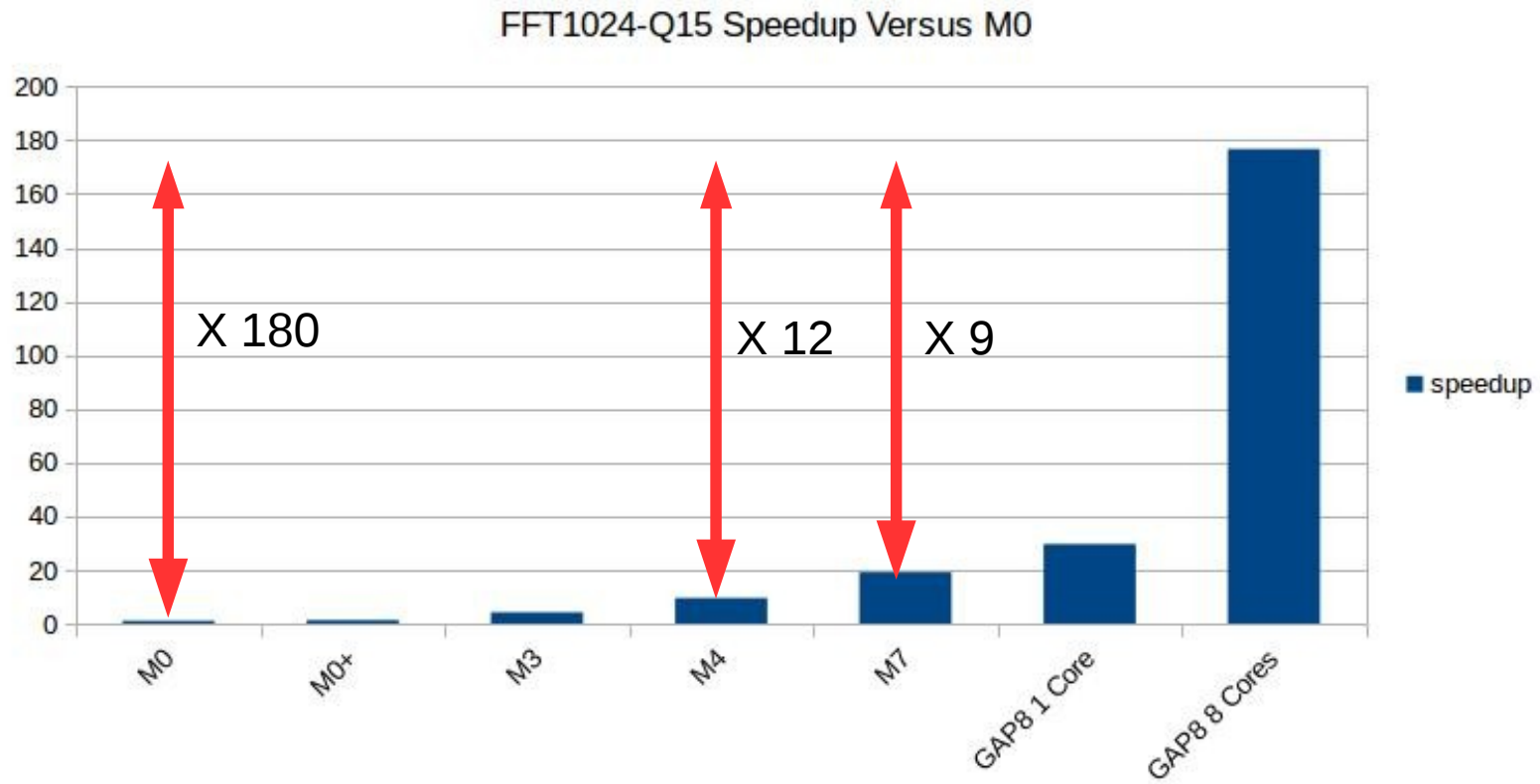
Number of operations (*,+,>>,Ld/St)

Number of Cycles running on 8 cores

FFT 256	FFT 1024	FFT 4096
11264	56320	225280

FFT 256	FFT 1024	FFT 4096
1167	4842	22710

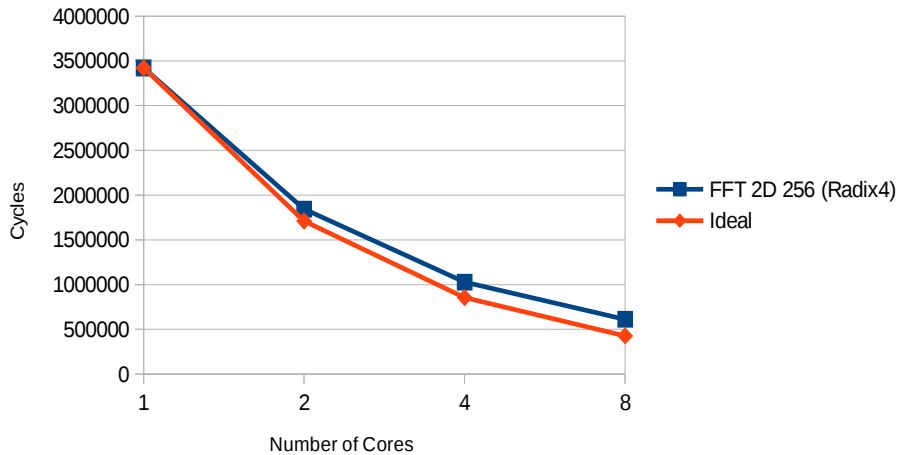
The work horse for radio, sound and vibration: FFT



ARM FFT1024 Q15 Data are with CMSIS optimized library

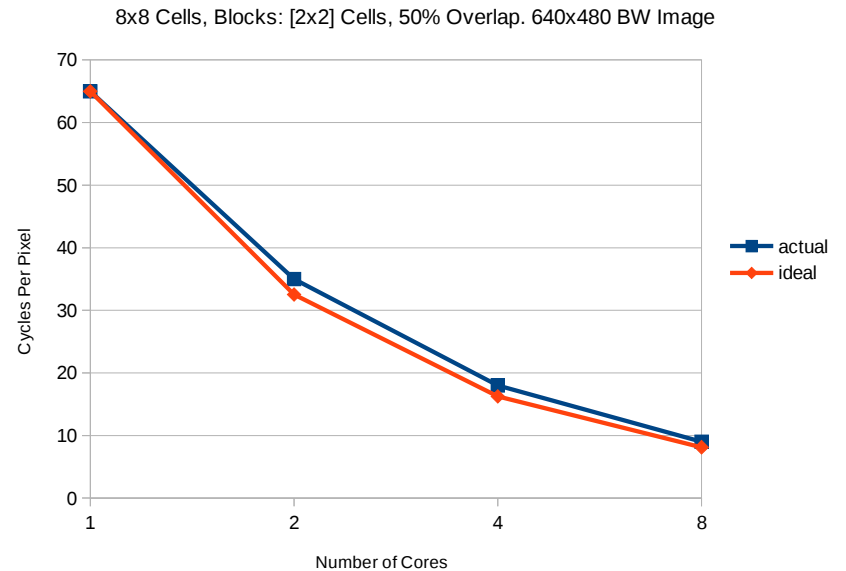
Visual Localization: FFT2D + HOG

FFT2D 256x256. Radix 4



1 384 000 cycles per image

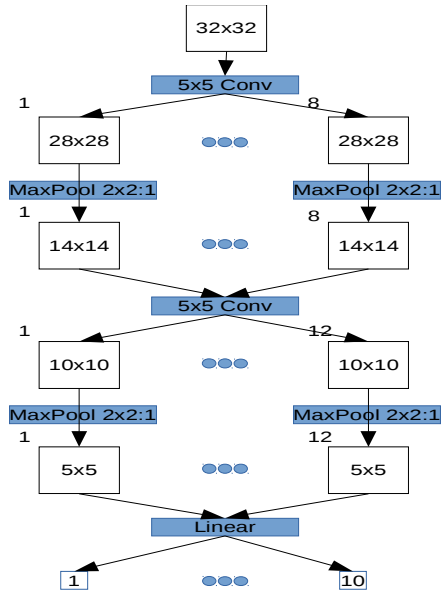
Histogram Of Gradients



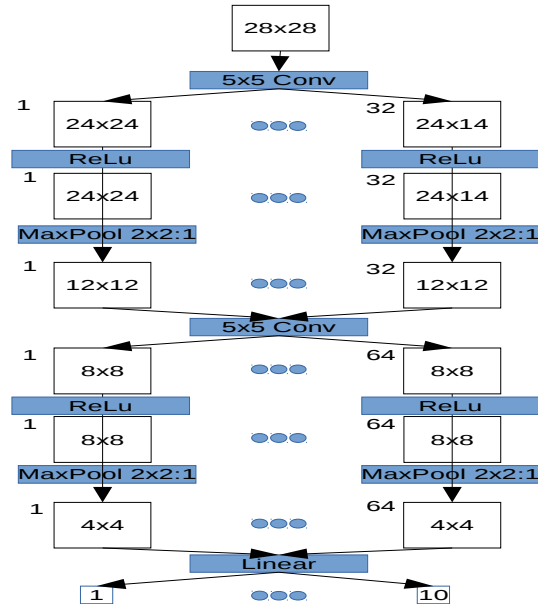
589 000 cycles per image

We need only 2 MHz per image

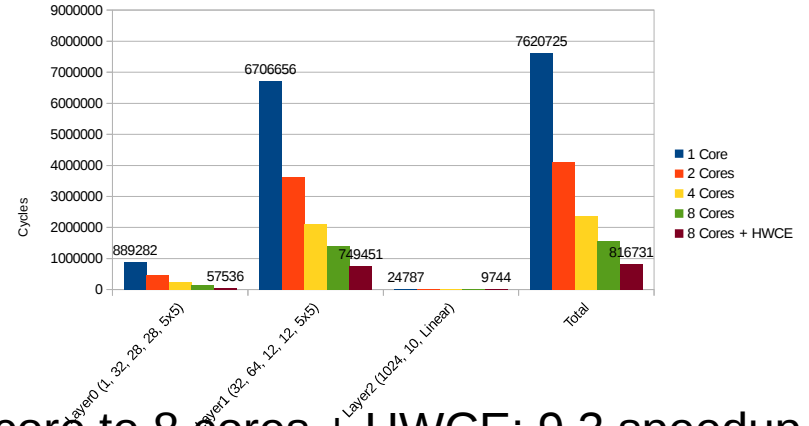
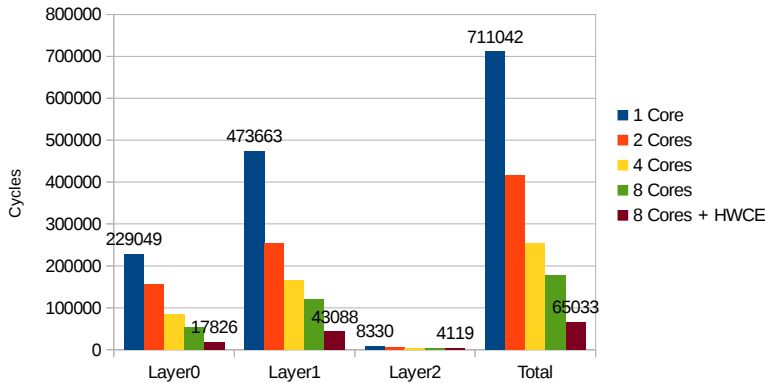
CNN based Image Classification



CIFAR10



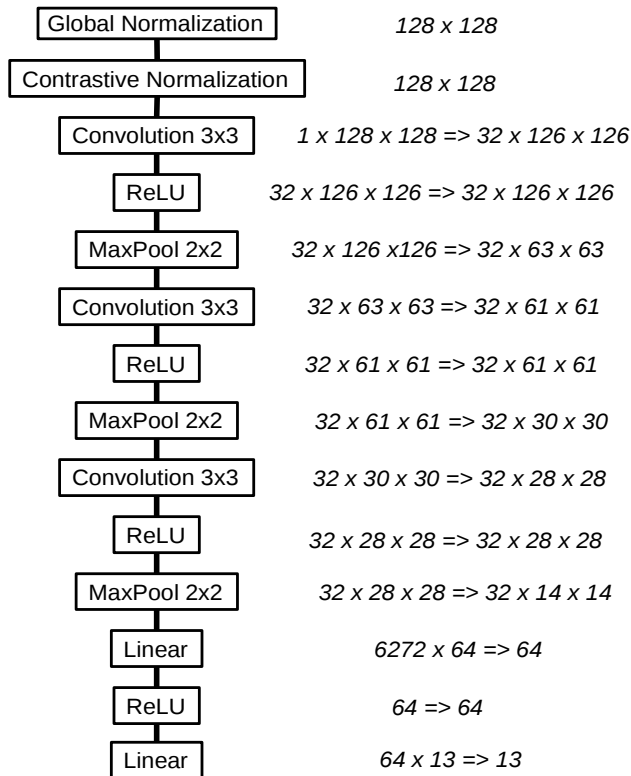
MNIST



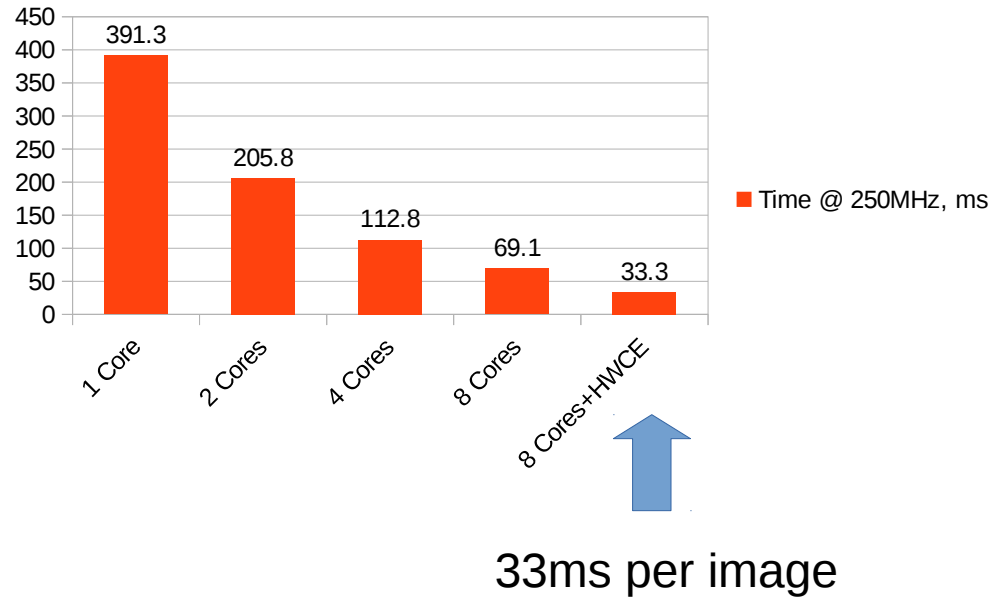
1 core to 8 cores + HWCE: 10.9 speedup

1 core to 8 cores + HWCE: 9.3 speedup

CNN based Image Classification



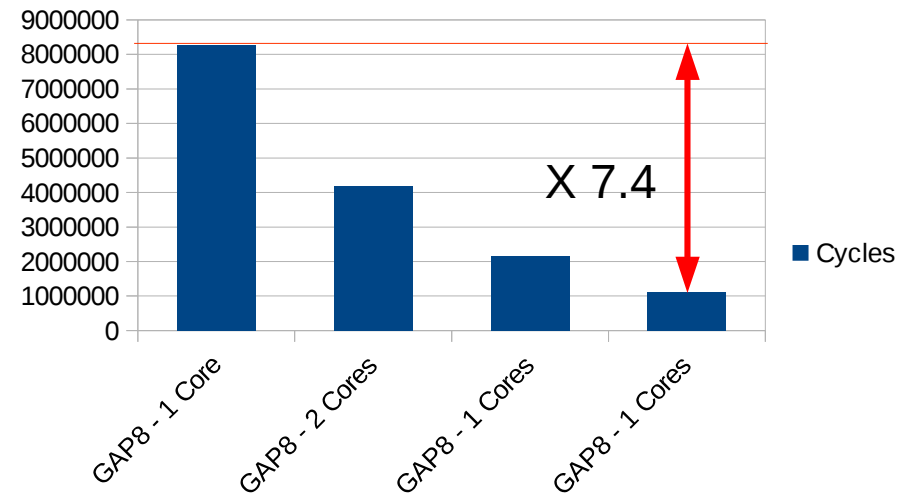
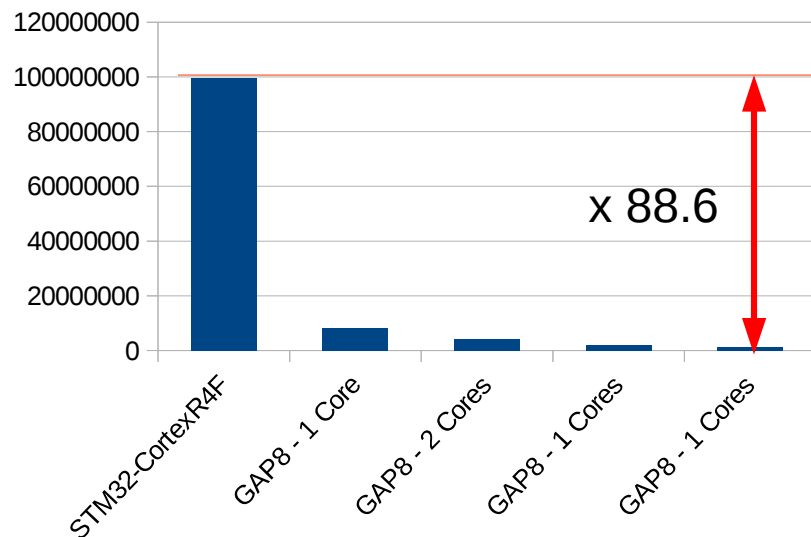
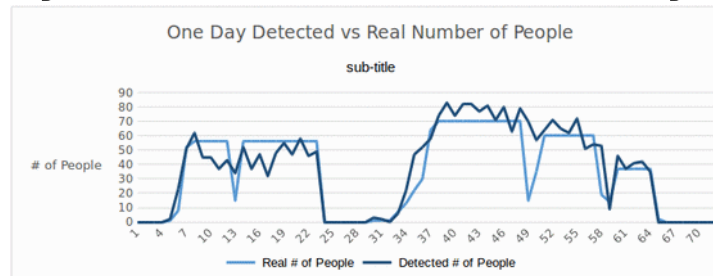
CNN 13 Layers, 128x128 Input, 14 Outputs



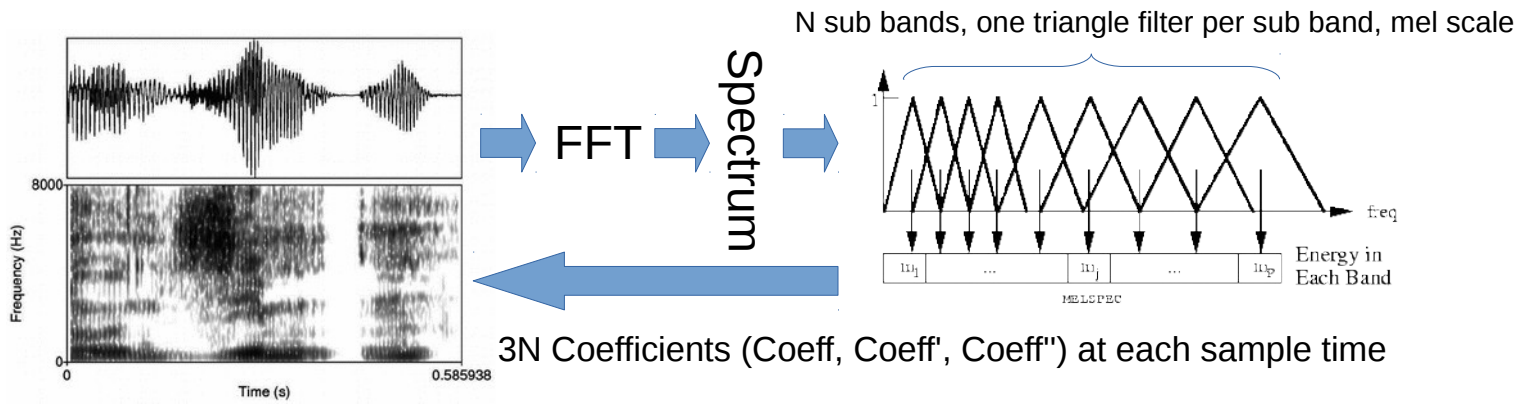
Trainable Par: 421 263
Neurons: 1 511 904

People Counting

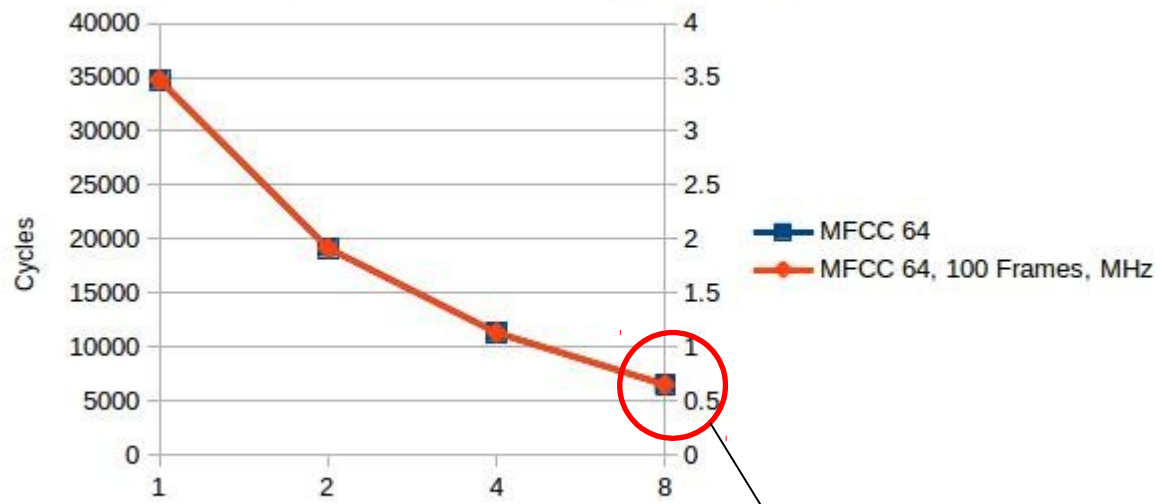
- Filtering + Difference of Gradient + SVM-RBF
- Open Space. Accuracy: approx 90%
- 1 Image every 3 minutes => 10 years on a battery



Audio Processing

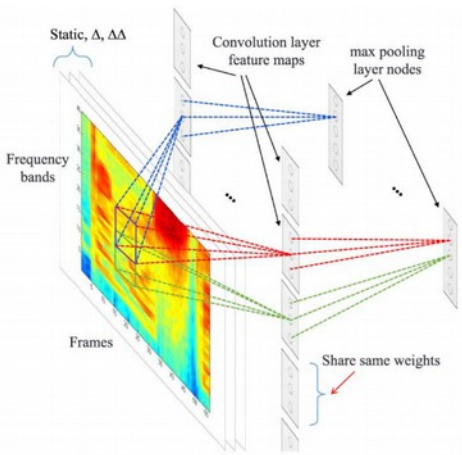
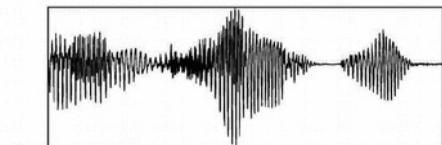


MFCC, 64 Bands, 16KHz/PCM16, 30ms Frame, 20ms Overlap



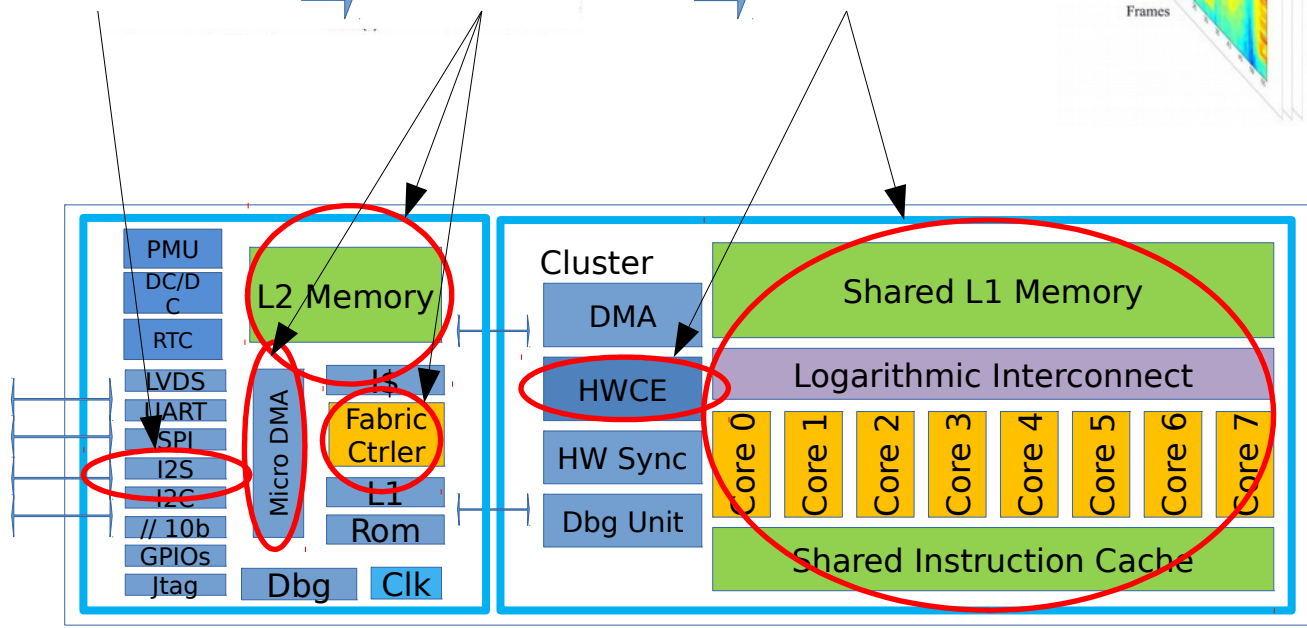
0.65 MHz on 8 Cores

Hierarchical Power Processing?



Gradually turn on resources

Sound ? → Phonem ? → Word ?



Conclusion

- GAP8 bridges the gap between ultra low power MCU and multi-core processor:
 - Smart sensing on data rich sensors achievable within tinny power budget: uW in Idle, mW in micro controller mode, 5-20mW in number crunching mode : Few Mops to up to 12Gops
 - Low cost bill of material
- GAP8 agile power management architecture combined with IOT low duty cycling is a perfect fit for FDSOI process