SoC Product Design with Body Biasing Using FD-SOI
基于FD-SOI工艺衬底偏置技术的SoC产品设计

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芯原控股有限公司
Agenda

- VeriSilicon and FD-SOI
  芯原与FD-SOI
- Deep Research and Product Design with Body-Bias
  衬底偏置技术的深入探索及产品设计
- Development in FD-SOI ECO-system
  芯原在FD-SOI产业生态上的推动
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VeriSilicon and FD-SOI
芯原与FD-SOI

▲ Kick off FD-SOI task force, since 2012

▲ Cosponsor of FD-SOI Forum, since 2013

2016 Shanghai FD-SOI Forum
VeriSilicon and FD-SOI
芯原与FD-SOI

▲ With STMicroelectronics on ST28nm FD-SOI

► Since 2013
► First PPA data and Body-Bias data
► “White box” license of IPs with modification rights
VeriSilicon and FD-SOI
芯原与FD-SOI

▲ With Samsung on SEC28nm FDS

► Since 2014
► Support Samsung 2015 DAC
► Tapeout 1st SEC28FDS in May, 2017
VeriSilicon and FD-SOI
芯原与FD-SOI

▲ With GlobalFoundries on GF22nm FDX

► Since 2015
► One of the earliest collaborators on GF22FDX
► 1st PPA data provider and 1st Library QA

<table>
<thead>
<tr>
<th>Date</th>
<th>Event Description</th>
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<tbody>
<tr>
<td>7/22</td>
<td>PDK V0.1_1.0 release</td>
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<tr>
<td>7/24</td>
<td>Starter kit release</td>
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<tr>
<td>7/27</td>
<td>PDK V1.2_2.0 release</td>
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<td>7/29</td>
<td>More cells with FBB and 0.4v flop cells release</td>
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<td>8/1</td>
<td>Invecas released 22DFX library with FFB for A7 run</td>
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<td>8/5</td>
<td>0.4V STD cell with 1v/2/-2v BB” based on q3v1 release</td>
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<td>8/17</td>
<td>PDK V0.2_0.0 release</td>
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<tr>
<td>8/19</td>
<td>Inv vecas released SLVT library with 0 bias for A7 @1.2Ghz run</td>
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<tr>
<td>8/23</td>
<td>Updated library release</td>
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<td>8/30</td>
<td>Inv vecas released LVT library with 0 bias for A7 @800Mhz run</td>
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<td>8/31</td>
<td>Training on PDK V0.1_1 and 22FDX</td>
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<td>9/8</td>
<td>A7 evaluation and device simulation</td>
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<td>9/10</td>
<td>GF14LPP STD libraries release</td>
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<tr>
<td></td>
<td>Scaled memory models for A7 release</td>
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<tr>
<td></td>
<td>TT@25C PVT with 0v/0v</td>
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Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

▲ Deep Research -- “Typical” Corner Setup Sign-off Technology

Explore The Possibility to Sign-off Setup at “TT”, for area sensitive case.

* Total Power = 70% Dynamic + 30% Static

** Test case use ARM Cortex-A7 running at 900Mhz.

![Graph showing area, leakage, dynamic, and total power comparisons between traditional slow-corner setup sign-off, typical-corner setup sign-off, and typical-corner sign-off + FBB trimming.](image-url)
Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

▲ Deep Research -- “Slow Corner + FBB” Setup Sign-off Technology

Explore The Possibility to Sign-off Setup at “SS + FBB”, for power sensitive case.

* Total Power = 70% Dynamic + 30% Static, enable all of the different Poly-Bias options.

** Test case use ARM Cortex-A7 running at 1Ghz.

![Graph showing Area, Leakage, Dynamic, and Total Power comparisons between Traditional Slow-Corner Setup Sign-off and Typical-Corner Setup Sign-off.](image)

- **Area**: 5% reduction for Typical-Corner Setup Sign-off
- **Leakage**: 30% reduction for Typical-Corner Setup Sign-off
- **Dynamic**: 25% reduction for Typical-Corner Setup Sign-off
- **Total Power**: 193.1 for Traditional, 139.7 for Typical-Corner Setup Sign-off

Legend:
- **Traditional Slow-Corner Setup Sign-off**
- **Typical-Corner Setup Sign-off**
Deep Research and Product Design with Body-Bias
衬衫偏置技术的深入探索及产品设计

▲ Deep Research -- PPA Big-Data Curve for Quick Library Selection

Body-Bias & Vth options are flexible knobs which can help 12-Track library to cover most of the application scenarios, with very few area penalty.

* Data are processed by normalization based on 800Mhz case.
Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

▲ Deep Research -- PPA Big-Data Curve for Quick Library Selection

Leakage Power increased fast in higher performance applications.

* Data are processed by normalization based on 800Mhz case.
GLOBALFOUNDRIES and VeriSilicon Holdings Co., Ltd. (VeriSilicon) announced a collaboration to deliver the industry’s first single-chip IoT solution for next-generation Low Power Wide Area (LPWA) networks based on GF22FDX.

1. Enable complete cellular modem module on a single chip

- RF radio
- NB-IoT & CAT-M1 Front-end
- Baseband
- Power Management IC
Product Design -- 1st Single-Chip Solution for Next-Gen IoT Networks

2. Power Efficiency Body-Bias & Low Power Structure

- **Reverse Body-Bias:** 10x lower leakage for Watchdog.
- **Forward Body-Bias:** High-performance and Low Dynamic Power for Baseband
- **Power-off:** RF and Baseband can be powered off in Standby Mode.
Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

▲ Product Design -- Implementation

► 1. Library Selection

Vth Selection:
- LVT + HVT, balance Dynamic Power and Leakage Power
- Single Vth in block, reduce OCV and avoid special Implant Placement Rule.

Body-Bias Selection:
- FBB: High-performance, Low Dynamic
- RBB: Low Leakage

![Diagram showing chip components such as RF, PMIC, DSP/AP/Baseband, Watchdog, etc. with Vth and Body-Bias selections indicated.]

15
Product Design -- Implementation

2. Bias Region Isolation

Isolation Requirement

- Different Bias Regions need to be isolated by Deep Nwell (S3)
- FBB and RBB cells cannot be mixed in the same Bias Region.
- Some IP may not support FBB/RBB, need to be isolated as well

Choose correct Boundary cell to isolate different regions.

- Edge Cell
- Corner Cell
- TOP or BOTTOM Cell
Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

Product Design -- Implementation

2. Bias Region Isolation

Isolation Physical requirement

- Different Bias Regions need to meet S3 DRC rule.
- No Standard Cell or M1 routing allowed between two different Bias Region.
Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

▲ Product Design -- Implementation

▶ 3. Bias Connection

UPF/CPF support

- IEEE 1801-2009 is used to define Bias domains for P&R
- Latest EDA tools support N-well/P-well connection.

```plaintext
pg_pin (VNW_N) {
    pg_type : nwell;
    physical_connection : device_layer;
    voltage_name : "VNW_N";
}

pg_pin (VPW_P) {
    pg_type : pwell;
    physical_connection : device_layer;
    voltage_name : "VPW_P";
}
```
Product Design -- Implementation

3. Bias Connection

TAP cell type
- *TAPZBX* support Zero Bias
- *TAPX* support FBB/RBB

TAP cell connection
- C1 (metal3) drop vias to TAP Bias Pin
- No need to be too wide

Bias Net Spacing Rule
- Need to consider High-Voltage spacing
  DRC rule because Bias Net Voltage range is (-2V, 2V)
Deep Research and Product Design with Body-Bias

衬底偏置技术的深入探索及产品设计

▲ Product Design -- Implementation

► 4. Bias Sign-off Criteria

PVT corner will change to PVT + Bias = PVTB

• **Static Body-Bias**, only need to sign-off at Chosen Bias Voltage:
  
  SS_0P72V_0P00V_XPXXV_MXPXXV_125C.lib  
  FF_0P88V_0P00V_XPXXV_MXPXXV_M40C.lib

• **Dynamic Body-Bias**, need to sign-off at both Zero-Bias and selected Bias Voltage, number of corners will be double:
  
  SS_0P72V_0P00V_0P00V_0P00V_125C.lib  
  FF_0P88V_0P00V_0P00V_0P00V_M40C.lib  
  SS_0P72V_0P00V_YPYYV_MYPYYV_125C.lib  
  FF_0P88V_0P00V_YPYYV_MYPYYV_M40C.lib

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<th>VDD</th>
<th>BIAS</th>
<th>Temp</th>
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<td>VDD-10%</td>
<td>V/-xV</td>
<td>-40C</td>
</tr>
<tr>
<td>SS</td>
<td>VDD-10%</td>
<td>xV/-xV</td>
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<td>VDD+10%</td>
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</table>
## Product Design -- Implementation

### 5. How to simplify Sign-off jobs?
- Sign-off different region as **Static Body-Bias**.
- Use **Single Vth** to reduce OCV.
- Keep enough timing margin at boundary.
- Choose representative simplified corner.
Deep Research and Product Design with Body-Bias
衬底偏置技术的深入探索及产品设计

▲ Product Design -- How to make it even easier?

Easy Design Flow Adoption

- Migration From 40nm/28nm bulk to 22FDX (Design Flow)
  - Digital Design Flow is similar to bulk digital design flow
  - Some of the features are for advanced nodes (both bulk and SOI)
    - AOCV/POCV/LVF – Double Patterning Extraction – In-design modules
    - The differences are taken care of in our Reference Flow releases
    - Can either use our Reference Flow or use it as blue print

Veri Silicon
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Development in FD-SOI ECO-system
芯原在FD-SOI产业上的推动

▲ VeriSilicon IP Platform and Design Service Platform (Both 28nm/22nm)

**IP Platform**

▲ Low Power Memory Compiler
低功耗存储器编译器

▲ AD/DA
模数/数模转换器

▲ AUDIO CODEC
音频编解码器

▲ USB3.0 Type-C PHY
USB 3.0 Type-C物理层

▲ MIPI DPHY (Main in Display transfer)
MIPI DPHY物理层

▲ DDR/LPDDR PHY
DDR/LPDDR物理层

▲ 1.25Gbps-12.5Gbps Serdes
面向有线通信的1.25Gbps-12.5Gbps多协议高速串联解串器

▲ BLE 5.0
蓝牙低功耗5.0

▲ NB-IoT IP
窄带物联网IP的研发 (22nm)

**Design Service Platform**

▲ FD-SOI Design Service
FD-SOI定制化设计服务
Development in FD-SOI ECO-system
芯原在FD-SOI产业上的推动

▲ Low Power Memory
Designed by VeriSilicon, Silicon Verified Low Power Memory

288K bit and 198K bit SRAM instance
Porting the same low power structure on 28nm FD-SOI and 22nm FD-SOI.
Dynamic Power reduced by 24% in 28nm FD-SOI and 45% in 22nm FD-SOI.

<table>
<thead>
<tr>
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<th>RASP 16384x18 Dynamic Power</th>
<th>RASP 2816x72 Dynamic Power</th>
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<tr>
<td>GF 28 SLP</td>
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<tr>
<td>SEC 28 FDS</td>
<td>0.76</td>
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<tr>
<td>GF 22 FDX</td>
<td>0.55</td>
<td>0.49</td>
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Development in FD-SOI ECO-system
芯原在FD-SOI产业上的推动

FD-SOI projects in 2017

SEC 28nm FDS
► U.S. customer, IoT application, low dynamic power.
► VeriSilicon designed IP involved, USB, POR, CODEC, MIPI.
► Tapeout in May 2017, wafer delivered, test ongoing.

ST 28nm FD-SOI
► China customer, high-performance application.
► Forward Body-Bias involved.
► Final run stage, target tapeout in Q4, 2017,

GF 22nm FDX
► U.S. customer, AI application.
► Complex CNN, and VeriSilicon powerful VIP inside.
► Target tapeout in Q4, 2017
Summary

▲ VeriSilicon and FD-SOI

An overall view about VeriSilicon and FD-SOI, how we began on FD-SOI and how we work with great foundry partners.

▲ Deep Research and Product Design with Body-Bias

Shared application approaches of Body-Biasing, demonstrated different sign-off corners with body-bias and big-data of library evaluation.

On the basis of NB-IoT collaboration chip, demonstrated how to do a Body-Bias chip.

▲ Development in FD-SOI ECO-system

Updated FD-SOI status in VeriSilicon, including IP Platform and Design Service Platform.