Philippe Flatresse, SOITEC

Philippe Flatresse received M.S. degree in Electrical Engineering in 1995 and PhD degree in Microelectronics in 1999 from Grenoble institute of technology. During his thesis, he has developed the LETISOI spice model dedicated to SOI technologies at CEA LETI, the R&D laboratory from French Atomic Energy Commission.

In year 2000, he joined STMicroelectronics Central R&D to deploy the SOI digital design within the company. He has developed the first SOI standard cells and SRAM libraries as well as IOs including innovative ESD solutions. He has also invented several dedicated CAD tools and low power digital design techniques such as power switches. Thanks to this work, he has pioneered the SOI technology and demonstrated its key advantages for low power high performance digital applications. As design architect, his current research interests are the convergence of high performance and low standby power towards automotive and IoT applications thru disruptive digital and analog aware design solutions like body biasing in FDSOI technology.

His expertise covers both bulk and SOI technologies, including electrical characterization, spice modeling, design of libraries, low power and high performance digital design techniques. He has authored or co-authored more than 70 technical papers in advanced CMOS technologies.