RBB & FBB in FDSOI

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Body Bias advantages

A key differentiator offering full flexibility in FD-SOI

- Performance boost
- Power optimization
- Process, T° and aging compensation
- Easy implementation
Extended Body Bias Range in UTBB FD-SOI

[Flatresse ISPLED 2014]
UTBB FD-SOI: Extended Body Voltage Range

- **RVT: Conventional Well (CW) - RBB**
  - NMOS
  - PMOS
  - Gndsn
  - Vddsp
  - p-Well
  - n-Well

- **LVT: Flip Well (FW) - FBB**
  - NMOS
  - PMOS
  - Gndsp
  - Gndsn
  - n-Well
  - p-Well

[Flatresse et al. ISSCC 2013]
Body Bias Efficiency - Silicon Benchmark

[Felloux-Prayer et al. S3S 2014]
Body Bias Usage – 6 different scenarios

Performance boosting

![Graph showing Total Power vs. Frequency with Body Bias (FBB) at 0.6V and 1.1V.]
Body Bias Usage – 6 different scenarios

- Performance boosting
- Power optimization

![Diagram showing total power consumption with different FBB voltages and frequencies.]

- Total Power
- FBB
- 0.6V
- 0.8V
- 0.9V

FBB
Body Bias Usage – 6 different scenarios

Performance boosting

Power optimization

Leakage saving
Body Bias Usage – 6 different scenarios

- Performance boosting
- Power optimization
- Leakage saving
- Area saving
Body Bias Usage – 6 different scenarios

- Performance boosting
- Power optimization
- Leakage saving
- Area saving
- P,T,A Compensation
- Or any combination …
**Body-Bias Product Use Case**

- **ULV** ➔ **Low power** ➔ **Best mW/MHz** ➔ **High performance**

* Benchmarked with respect to noBB

Courtesy STMicroelectronics
Body Bias - Key deployment steps

- Product specification
- Body Bias IPs & Architecture
- Design implementation
- Silicon engineering
(Vdd, PB, BB) choice becomes a power-delay trade-off exercise.
Built-in Body Bias in your design flow is key!

- **ARM Processor**
  - Target frequency: 1GHz @ WC/0.85V
- **Two FD-SOI implementations comparison**
  - Standard WC methodology
  - SS corner compensated with 600mV FBB

<table>
<thead>
<tr>
<th>Sign-off</th>
<th>Standard</th>
<th>Built-in BB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>1</td>
<td>0.95x</td>
</tr>
<tr>
<td>Total Power</td>
<td>1</td>
<td>0.75x</td>
</tr>
</tbody>
</table>
  - @ Vmax, 125C, RCmax     |
| Leakage                   | 1        | 0.7x        |
  - @ Vmax, 125C            |

*Courtesy STMicroelectronics*
FBB “Process Compensation” principle

<table>
<thead>
<tr>
<th>CORNER</th>
<th>BB</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>0.0V</td>
</tr>
<tr>
<td>TT</td>
<td>0.3V</td>
</tr>
<tr>
<td>SS</td>
<td>0.6V</td>
</tr>
</tbody>
</table>

FBB (to accelerate transistors speed)

Slow part: Frequency, Power and area Gain

Fast parts unchanged
Body Bias - Key deployment steps

- Product specification
- Body Bias IPs & Architecture
- Design implementation
- Silicon engineering
Body-Bias Generator – a key IP

• Fully integrated generator for the NMOS/PMOS body voltage generation

• 50/100 mV FBB steps up to 1.8 V

• Charging and discharging well capacitances, challenge –Vss

• Switched capacitors generate negative bias and pump substrate

[Blagojevic et al. VLSI 2016]
IP requirement for Body-Bias

- BBgen
- On Chip Sensors
- Voltage sensor
- Temperature sensor
- OTP memory
- FBBmin + NvsP search algo
Body Bias compensation Type vs VDD

[Manchester et al. TCAS 2017]
Body-Bias Architecture Selection

<table>
<thead>
<tr>
<th>Open loop with Off-chip BBG</th>
<th>Open loop with On-chip BBG</th>
<th>Closed loop with On-chip BBG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Regulator</td>
<td>BBGEN</td>
<td>BBGEN</td>
</tr>
<tr>
<td>Body-Bias Island</td>
<td>Body-Bias Island</td>
<td>Body-Bias Island</td>
</tr>
<tr>
<td>Sensors</td>
<td>Sensors</td>
<td>Sensors</td>
</tr>
<tr>
<td>• For &gt;0.9V</td>
<td>• For &gt;0.9V</td>
<td>• For full voltage range</td>
</tr>
<tr>
<td>• FBB/Power</td>
<td>• FBB/Power/Process Comp.</td>
<td>• FBB/Power/PTA Comp</td>
</tr>
</tbody>
</table>
Body Bias - Key deployment steps

- Product specification
- Body Bias IPs & Architecture
- Design implementation
- Silicon engineering
Process compensation with Body Bias Implementation example

- Multi-cores running @1GHz
- Complexity ~50M gates
- Body Bias Area: 80%
- Power Supply 0.9V – Temp Inversion

![Diagram with BBGen, On Chip Monitors, OTP, V/T Sensor]
Body Bias - Key deployment steps

- Product specification
- Body Bias IPs & Architecture
- Design implementation
- Silicon engineering
FBB “Process Compensation” calibration

Production Test at ST (EWS)
- Begin EWS
- Search BB
- Store BB in OTP
- End EWS

Optimal Body Bias level is defined Die by Die depending on Speed/Power characteristic measured on “on chip monitors”

Application (at Boot)
- Start-up
- Read OTP BB
- Set BB
- Normal operation

Optimal Body Bias level is stored in One Time Programmable memory THEN Read at Boot

An Embedded circuit (Body Bias Generator) set that Bias level
VBB min Search

Begin

VDD, temp VBBmax, Ftarget

VBBN=VBBP min search

NMOS vs PMOS VBB offset calculation

+/− 1 or 2 VBB step Final adjust

Store VBBN, VBBP

end

- VDD and Temp condition for calibration
  Algorithm setting via frequency target and max allowable VBB

- Algorithms to find common VBBN/VBBP, only used at EWS and start-up

- NMOS and PMOS separate measurement

- Final VBBN and VBBP adjust by +/− 1 or 2 step; Guaranties minVBB with F >Ftarget

- Stored in OTP for EWS calibration then in BBgen register for others
The future is body bias adaptive!

Adaptive voltage control will also be used to maximize performance and yields.

Dynamic Body-Bias for P, T, A compensation

[Flatresse NEWCAS 2015]
Adaptive Body-Bias for Aging compensation

- Progressive degradation modes (BTI, HCI, TID) are captured by canary FF solutions
- Compensation through ABB is possible under real-time conditions

[Mhira et al. IRPS 2017]
PULPv3 SoC – RVT Conventional well

- PULP: Parallel Ultra-Low-Power Platform
  - 4-cores near-threshold processor
- Frequency Range:
  - 20 MHz @ 0.5V - 200 MHz @ 0.7V
- On-Chip Body Bias Generator
  - Average power: 4,15 µW
  - Body Bias Range: -1.5V to 0.4V
RVT-based design with Body-Biasing
Key flavor for IoT

Figure of merit @ 0.5V Vdd

- FBB 0.5V $\leftrightarrow$ 160% Higher Freq
- RBB -1.8V $\leftrightarrow$ 10X Less Leakage

[Rossi, HCS 2015]
PULP: RBB/FBB frequency boosting

Body Bias varying from -1.0V to +0.5V

- Frequency
- Body Bias
- Leakage

300Mhz
100Mhz
0.5V FBB
-1.0V FBB
3000 µA
30µA
FDSOI & Body Biasing - Take away

› True back gate solution for ultimate Vt control
› Built-in Body Bias in the design is key, easy to implement!
› Up to 200% performance boost and 10X leakage reduction at low voltage
› Significant Vddmin reduction, leading to power saving and reliability relaxation
› Variability spread reduction
› FDSOI offers unique Body Bias control loop solutions for P,T,A compensation
› Enabling/Disabling BB allows to create several product variants
Thank you!