TRAINING DAY ON ANALOG, RF, HIGH SPEED, MILLIMETER WAVE AND MIXED-SIGNAL DESIGN TECHNIQUES IN FD-SOI TECHNOLOGIES

In the frame of the SOI Consortium Symposium

Santa Clara, April 27h, 2018

Organizer: Andreia Cathelin, STMicroelectronics

Mentors: Carlos Mazuré and Giorgio Cesana, SOI Industry Consortium

World renowned professors and experts from industry will deliver a series of four training sections of 1.5hrs each, dedicated to energy efficient and low power low voltage design techniques for analog, RF, high-speed, mmW and mixed-signal design.

Attendees will learn about design techniques that take full advantage of the unique features of FD-SOI, including body biasing capabilities that further enhance the excellent analog/RF performances of these devices.

Each section of this training day will take the participants through concrete design examples that illustrate new implementation techniques enabled by FD-SOI technologies and 28nm, 22nm nodes and beyond.

The design examples will cover basic building blocks through SoC implementations. A global Q&A session will close the day.

7.30 – 8.30: breakfast and registration

8.30- 10.00 Andreia Cathelin, Fellow, STMicroelectronics Crolles, France

FDSOI specific design techniques for analog, RF and mmW applications

Abstract: This course will first present a very short overview of the major analog and RF technology features of 28nm FDSOI technology. Then we will focus on the benefits of FD-SOI technology for analog/RF and millimeter-wave circuits. Design examples such as analog low-pass filter, inverter-based analog amplifiers and 30GHz and 60GHz Power Amplifiers, as well as mmW oscillators are given. A special focus will be done on the advantages of body biasing and special design techniques offering state of the art performance.

10.00 – 10.15: coffee break

10.15 – 11.45 Frank Zhang, Principal Member of Technical Staff, Globalfoundries

Circuit Design Techniques in 22nm FD-SOI for 5G 28GHz Applications

Abstract: This course will focus on taking advantages of FD-SOI's high frequency performance at relatively low current density to design high performance RF/mmWave circuits. Examples circuits include a 28GHz LNA, a 28GHz PA and an RF switch for 5G applications. The FD-SOI advantages such as low capacitance, high breakdown voltage and high output impedance will be exploited in these design examples. This course will also discuss how to extend these techniques to applications to higher frequencies and/or higher current densities that are subject to extreme temperatures and EM requirements.

11.45 – 13.00: lunch

13.00 – 14.30: Bora Nikolic, Professor, UC Berkeley, Berkeley, USA

Energy-Efficient Design in FDSOI

Abstract: This talk presents options for energy-efficient mixed-signal and digital design in FDSOI technologies. Effective generation of body bias and its use to improve efficiency will be presented on the examples of RF and baseband building blocks, temperature sensors, data converters and voltage regulators. The techniques will be presented within a concept of a RISC-V-based SoC, designed to operate in a very wide voltage range utilizing 28nm FDSOI.

14.30-14.45: coffee break

14.45 – 16.15: Sorin Voinigescu, Professor, University of Toronto, Toronto, Canada

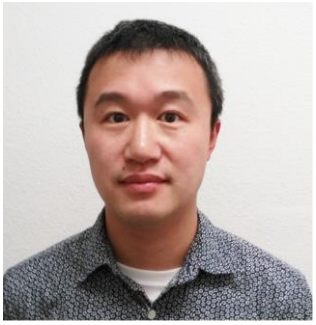
mm-Wave and Fiber-optics Design in FD-SOI CMOS Technologies

Abstract: This lecture will cover the main features of FD-SOI CMOS technology and how to efficiently use its unique features and suitable circuit topologies for mm-wave and broadband SoCs. I will overview the impact of the back-gate bias and temperature on the measured I-V, transconductance, fT, and fMAX characteristics and compare the maximum available gain, MAG, of FDSOI MOSFETs with those of planar bulk CMOS and SiGe BiCMOS transistors through measurements up to 325 GHz. Next, biasing, sizing and step-by-step design examples will be provided for VCO, doubler, switches, PA, large swing optical modulator drivers and quasi-CML circuit topologies and layouts that make efficient use of the back-gate bias to overcome the limitations associated with the low breakdown voltage of 20nm and 12nm FDSOI CMOS technologies.

16.15 – 17.00: General Q&A session and closing remarks

About the instructors:

Andreia Cathelin is Technology R&D Fellow with STMIcrolectronics in Crolles, France. She started electrical engineering studies at the Polytechnic Institute of Bucarest, Romania and graduated with MS from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France in 1994. In 1998 and 2013 respectively, she received PhD and "habilitation à diriger des recherches" (French highest academic degree) from the Université de Lille 1, France. Since 1998, she has been with ST, where her focus areas are in the design of RF/mmW/THz and ultra-low-power circuits and systems. She is the key design scientist in the promotion of all advanced CMOS technologies developed in the company and has an active participation in the frame of the SOI Consortium, an industrial group federating SOI technologies ecosystem. Andreia has had numerous responsibilities inside the IEEE community since more than 10 years. At ISSCC, she has been the RF sub-committee chair from 2012 to 2015, and since 2016 is the Forums Chair and member of the Executive Committee. She is member of ESSCIRC TPC since 2005. Since September 2013, Andreia is on the Steering Committee of ESSCIRC-ESSDERC conferences, where she has been the Chair from 2015 to September 2017. She has served different positions on the Technical Program Committees of VLSI Symposium on Circuits from 2010 till 2016. Andreia has authored or co-authored 130+ technical papers and 7 book chapters, and has filed more than 25 patents. Andreia is a co-recipient of the ISSCC 2012 Jan Van Vessem Award for Outstanding European Paper and of the ISSCC 2013 Jack Kilby Award for Outstanding Student Paper. She is as well the winner of the 2012 STMicroelectronics Technology Council Innovation Prize, for having introduced on the company's roadmap the integrated CMOS THz technology for imaging applications.



Frank Zhang received the B.E. and M.S. degrees in electrical engineering from the Cooper Union for the Advancement of Science and Art, New York, NY, in 2000 and 2001, respectively. He received the Ph.D. degree in electrical engineering from Columbia University, New York, NY, in 2008. He has been a Principal Member of Technical Staff at Globalfoundries since 2015, where he has designed integrated circuits using the 22nm FD-SOI process targeting applications in WLAN, 5G cellular, and automotive radar. He has previously worked on RF transceiver circuits for Icera/Nvidia (2011-2015), Texas Instruments (2008-2011), and Motorola (2001-2003). He was the recipient of the Best Student Paper Award from the 2008 IEEE RFIC Symposium.

Sorin P. Voinigescu holds the Stanley Ho Chair in Microelectronics and is the Director of the VLSI Research Group in the Electrical and Computer Engineering Department at the University of Toronto. He is an IEEE Fellow and a world renowned expert on millimeter-wave and 100+Gb/s integrated circuits and atomic-scale semiconductor device technologies. Between 1994 and 2002 he was first with Nortel Networks and later with Quake Technologies in Ottawa, Canada. In 2008-2009 and 2015-16, he spent sabbatical leaves at Fujitsu Laboratories of America, Sunnyvale, California, at NTT's Device Research Laboratories in Atsugi, Japan, and at Robert Bosch GmbH in Germany, exploring technologies and circuits for 128GBaud fiber-optic systems, 300Gb/s mm-wave radio transceivers, and radar sensors.

Dr. Voinigescu co-founded and was the CTO of two fabless semiconductor start-ups: Quake Technologies and Peraso Technologies. He was a member of the ITRS RF/AMS Committee, of the ExCom of IEEE CISICS, and is a member of the ExCom of the IEEE BCTM. He received NORTEL's President Award for Innovation in 1996 and is a co-recipient of the Best Paper Award at the 2001 IEEE CICC, the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won numerous Best Student Paper awards, most recently at IEEE IMS 2017. In 2013 he was recognized with the ITAC Lifetime Career Award for his contributions to the Canadian Semiconductor Industry.

Borivoje Nikolić is the National Semiconductor Distinguished Professor of Engineering at the University of California, Berkeley. He received the Dipl.Ing. and M.Sc. degrees in electrical engineering from the University of Belgrade, Serbia, in 1992 and 1994, respectively, and the Ph.D. degree from the University of California at Davis in 1999.
His research activities include digital, analog and RF integrated circuit design and communications and signal processing systems. He is co-author of the book Digital Integrated Circuits: A Design Perspective, 2nd ed, Prentice-Hall, 2003. Dr. Nikolić received many awards in his career, including the NSF CAREER award in 2003, and the best paper awards at the IEEE International Solid- State Circuits Conference, Symposium on VLSI Circuits, IEEE International SOI Conference, European Solid-State Circuits Research Conference, European Solid-State Device Research Conference, S3S conference and the ACM/IEEE International Symposium of Low- Power Electronics. Dr Nikolic is an IEEE Fellow.