



Applied Materials 300mm FEOL Products Status for RF-SOI

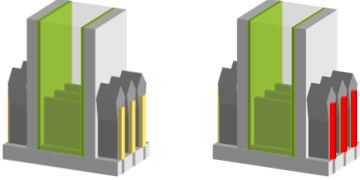
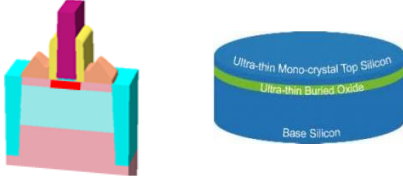

SPG / Front End Product (FEP) Group.
Papo Chen, Ph.D.

International RF-SOI Workshop, Shanghai, China, 19 Sept 2018

Outline

- **Technology Trend Overview: Logic vs. FD-SOI / RF-SOI**
- **Applied FEP Product Focus on FD-SOI & RF-SOI**
- **Summary**

Technology Trend Overview: Logic vs. FD-SOI / RF-SOI

Device	Logic	SOI	
Architecture	FinFET / Alternative Channels	FD-SOI / Alternative Channels	RF-SOI / Trap-Rich Layer
			
Challenges	<ul style="list-style-type: none"> ▪ SDE challenge, Lg/EOT Scaling ▪ Rc Reduction ▪ Recess S/D Epi control & preclean ▪ Dual Channel formation ▪ Gate Stack for SiGe Chnl ▪ Low-k Spacer 	<ul style="list-style-type: none"> ▪ SDE challenge ▪ Rc Reduction ▪ Raised S/D Epi control & preclean ▪ SiGe channel Epi control ▪ Gate Stack fabrication 	<ul style="list-style-type: none"> ▪ RF leakage through Sub ▪ Parasitic capacitances by sub or transistor
Approaches	<ul style="list-style-type: none"> ▪ Epi extension ▪ High activation highly doped films ▪ HKMG ALD films densification 	<ul style="list-style-type: none"> ▪ Epi extension ▪ High activation highly doped films ▪ HKMG ALD films densification ▪ SiGe for LNA performance boost 	<ul style="list-style-type: none"> ▪ High resistivity Epi layer ▪ Trap-rich Epi layer
Epitaxy	<ul style="list-style-type: none"> ▪ RP Epi with LT capability ▪ New Pre-Epi Cleans 	<ul style="list-style-type: none"> ▪ RP Epi with LT capability ▪ New Pre-Epi Cleans 	<ul style="list-style-type: none"> ▪ ATM Epi
Gate/PME/Oxidation	<ul style="list-style-type: none"> ▪ DPN3 / DPx ▪ RadOx (ISSG) 	<ul style="list-style-type: none"> ▪ DPN3 / DPx ▪ RadOx (ISSG) 	

Logic learning can benefit FD-SOI & RF-SOI developments

Applied Materials: Front End Products (FEP) Portfolio

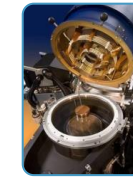
Process	Application Area	Product(s)
Oxidation	Thermal Oxidation/PME	RadOx → RadOx w/ CIP
	Plasma Oxidation/PME	Centura DPO
	Remote Plasma Oxidation/PME	Centura RPO



▪ Centura RadOx



▪ Vantage RadOx

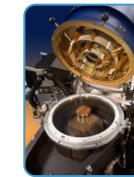


▪ Centura DPO



▪ Centura RPO

Process	Application Area	Product(s)
Gate	Plasma Nitridation/PME	DPN/DPN+ → DPN3 → DPx
	Thermal Nitridation/PME	RTx / Vulcan+ / Astra DSA w/ CIP



▪ Centura DPN/DPx



▪ Centura RTx



▪ Radiance Vulcan



▪ Astra DSA

Process	Application Area	Product(s)
Anneal	Soak / Spike	Rad/Rad+ → Vulcan/Vulcan+
	mSEC	Astra DSA → Astra DSA w/ CIP
	Low-Temp/High Productivity	Producer Anneal



▪ Radiance Vulcan



▪ Radiance



▪ Astra DSA



▪ NLA



▪ Producer Pyra

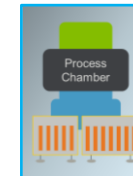
Process	Application Area	Product(s)
Epitaxy	Reduced Pressure	RP Epi → RP Epi w/ CIP / New Precursor
	Pre-Epi Clean	Siconi → Next-Gen Pre-Epi Clean
	Atmospheric	ATM Epi → ATM Epi w/ CIP



▪ RP Epi
▪ ATM Epi




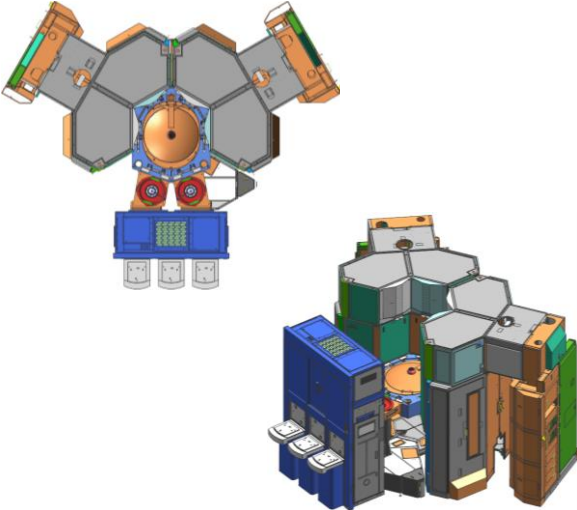

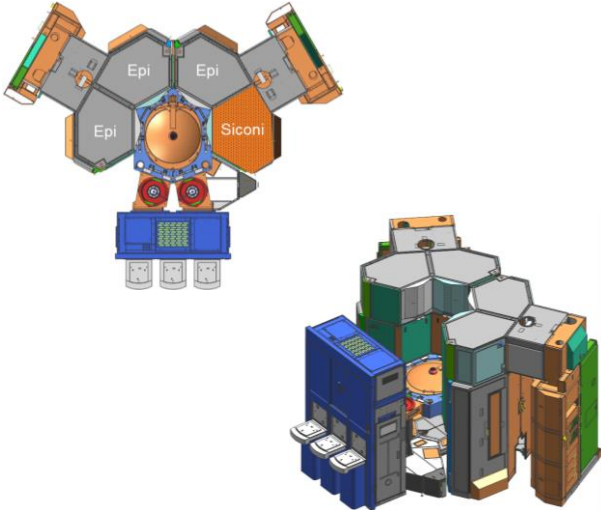
▪ Siconi



▪ New Preclean

Material Engineering – New Material / Alloy Deposition – Process Innovation

Applied Epi Configuration Options (Single vs. Dual ACP)

Single Centura ACP with Two Epi Chambers (Optional 1 or 2 Preclean)	Single Centura ACP with Four Epi Chambers (No Preclean need)	Dual Centura ACP with Four Epi and Two Preclean Chambers	Single Centura ACP With Odd # Epi Chambers & Preclean (3+1)
			
<p>40/32/28/22/20/16/14/10/7/5 nm Foundry/Logic. Wafer Epi (no preclean)</p>	<p>40/32/28/22/20/14/10/7/5 nm Foundry/Logic (moment preclean N/A) DRAM/3D NAND, Si Power Device</p>	<p>40/32/28/22/20/16/14/10/7/5 nm Foundry Logic 5nm cSiGe (preclean improve defect by “orders”)</p>	<p>New Available Configuration</p>
<p>Flexible, Small Footprint</p>	<p>Efficient Footprint, CoO, HT baking allowed.</p>	<p>Efficient CoO, Preclean Redundancy</p>	<p>Flexible, Small Footprint. Higher Tput / ft² with preclean</p>

Module platform provides flexible configuration options for Every Manufacturing Need

Summary

- *Applied's commitment:*
- Enable **Process Innovation** to support SOI development.
- Offer products **Beyond performance, Advance in Productivity and Reliability.**





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