I-fuse™ for FD-SOI:
Ultra-high reliability and Ultra-low Power OTP

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OTP Applications

- OTP: One-Time-Programmable Memory
  - Programmable **only once** to store **permanent** data
  - Allows each IC to be customized after fabrication, no costs
    - Every chip needs OTP, if available, affordable, & reliable

- Product feature selection
- 3D IC repair
- Memory repair (replace laser fuse)
- Device trimming / calibration (eliminate EEPROM)
- MCU code storage (replace flash)

- Chip ID, Security Key, IoT
Different OTP Technologies

- **Store data** Permanently **but Program Once**
  - NVM device

- **NVM mechanisms**
  - Break fuse, Rupture oxide, or trap charges in floating gates

- **NVM reliability**
  - 10x to 100x lower than logic devices

- **Revolutionary fuse-base OTP to overcome all problems**

![Diagram of eFuse, Oxide rupture, and Floating-gate]

- Break fuse
  - Explosive
  - ≤0.18um
  - Grow back
  - 29ppm defect

- Rupture oxide
  - Explosive
  - ≤ 0.18um, ≥14nm
  - Self-healed
  - 10ppm defect

- Trap charges
  - Statistical
  - ≥0.35um, ≤0.6um
  - data retention
  - 100ppm defect
I-Fuse™ vs. Efuse Programming

- **I-fuse™**: orderly program; Guaranteed reliable by physics
- **eFuse**: explosive program => create debris => grow back

Critical current: **Onset of Thermal runaway** ($Q_{\text{GEN}} > Q_{\text{LOSS}}$)

**Power devices should not operate in thermal runaway. So programming a fuse should not.**
Why Non-breaking Fuse?

Many advantages for non-breaking fuses:
- => low program voltage => **No charge pump requirement**
  => Uses standard logic design/test flow
- => low program current => smaller size
  => lower power
- => control program => **tight post-program resistance distribution**
  => higher reliability
- => less damage => sustain high temperature
  => higher data security
- => electro-migration => no debris after program => no grow back

Applications:
- Low voltage/current program/read: 0.7um to 14/10/7nm
- High quality, reliability: IoT, Automotive, Industry, communication

*Only OTP programming mechanism that can be modeled by physics: heat generation/dissipation and electro-migration*
Efuse vs. I-Fuse™

- Revolutionary I-fuse™ fixes all problems in eFuse
- Reliability & qualification guaranteed by physics, not engineering

<table>
<thead>
<tr>
<th></th>
<th>Efuse*</th>
<th>I-fuse™</th>
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<tr>
<td>28nm and beyond</td>
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<tr>
<td>Program current</td>
<td>Up to 100mA</td>
<td>&lt;3mA</td>
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<td>HTS qual</td>
<td>4Kb passed 125°C 1Khr with 2 cells per bit</td>
<td>256Kb passed 250°C 1Khr without any redundancy</td>
</tr>
<tr>
<td>Read time in life</td>
<td>&lt; 1sec</td>
<td>Unlimited read time</td>
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<tr>
<td>Program yield</td>
<td>A few % loss</td>
<td>~100%</td>
</tr>
<tr>
<td>Scalability</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Testability</td>
<td>NO</td>
<td>YES, ZERO defect</td>
</tr>
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* Customers testimonies
Why FD-SOI?

- Want a phone as small as a watch?
- You need FD-SOI
  - RF integration (multi-band/mode)
    - Low loss, high linearity, low parasitic cap, FBB/RBB etc.
  - Small form-factor
  - Ultra-low power (e.g. 0.4V/1μA)
  - Low costs
- I-fuse™ more advantages to FD-SOI: low breakdown voltages!!

1900s 1950s 1970s 2000s 2020s
I-Fuse™ 4K8 Array at 22nm FD-SOI

- **4K8 I-fuse™ Array:** (S3S Conf ‘17)
  - Small 1R1T cell: 0.744um²
  - Small 4K8 array: 0.0312mm²
  - 0.9V~1.4V program voltage
  - <1.4mA program current
  - High data security
  - High reliability: 150°C 1Khr HTS

- **4K8 I-fuse™ Macro:** (S3S Conf Oct. ‘18)
256Kb I-Fuse™: 250oC HTS 1Khr

- 300oC, 4,290hr HTS proven high reliability in mature nodes
  - I-fuse™ passed 300oC, 4,290hr HTS. 0 defect in 3Mb (VIS 0.16 HV)
  - I-fuse™ passed 400oC, 8hr HTS. 0 defect in 3Mb (VIS 0.16 HV)
  - eFuse can’t pass 400oC, 2hr HTS. 20-30 defects in 1Mb

- 250oC HTS, 1Khr 256Kb I-fuse™ Macro on 22nm FD-SOI
  - 250oC, 1,000hr HTS PASSED. 0 defect in 10s Mb
  - No visible I-fuse™ resistance changed. No tailing bits

- 125oC HTOL, 1Khr I-fuse™ Macro on 22nm FD-SOI
  - 125oC, 1,000hr HTOL PASSED. 0 defect in 10s Mb
  - No visible I-fuse™ resistance changed. No tailing bits.
  - Unlimited Read time: at least 100x read and cycle time of eFuse
  - To be announced with foundry soon & in IEEE conference
  - Can not disclose more because of pre-publication
0.4V/1uA Read @22nm FD-SOI

- Battery-less RFID need 128b OTP for authentication
  - Low voltage: 0.4V, rectified from antenna receiver (0.8V VDD)
  - Low power: 1uW, source power from weak antenna coupling
  - High reliability: secured key stored in OTP for authentication

- I-fuse™: the only OTP in the world to meet the goals
  - 64x1 I-fuse™ OTP worked 0.4V/1uA @22nm FD-SOI !!
  - Cell: low voltage programmable allows operating in 0.4V
  - Peripheral => 0.4V/1uW Sense Amplifier:
    - Not MOS as amplifier. Need to bias in high gain region
    - Not Inverter as amplifier. Need post-program resistance >100K ohm
    - Novel circuit techniques never used in memory designs before

- To be announced w/ foundry and European research Institute soon
- To be published in IEEE conference
- Can not disclose more because of pre-publication
I-Fuse™ in Standard Cell Library

- **Build I-fuse™ bit-slice in any standard cell library**
  - Meet standard cell library formats and design/layout guidelines
  - Simple R/W interface, just like SRAM
  - Write Verilog model to build any low bit-count I-fuse™ OTP
  - Synthesize and P&R I-fuse™ OTP with the rest of circuits

- **New Applications: local variations tuning**
  - Store FBB/RBB bias data for local tuning in each macro
    - Unique FD-SOI features to trade performance vs. leakage
  - Store wordline pulse width data in each 256Kb tile for 4Mb
    - Reduce wordline width in fast corner to save power in each tile
    - Can save up to 30% of 4Mb SRAM current consumption
  - OTP key built by random logic more secured than OTP memory

- **Pre-requisite**
  - I-fuse™ program voltage/current are in-line with any logic circuits
  - I-fuse™ needs no high voltage, and no charge pumps
  - I-fuse™ allows simple SRAM-like I/F, as reliable as any logic devices
I-Fuse™: ZERO Defect

- Field return is very costly
  - 10x costs from wafer sort, packaged chip, module, PCB, to system
- ZERO defect after shipping
  - Defects should be found out and screened before shipping
- I-fuse™ can achieve ZERO defect
  - OTP dilemma: fully tested before shipping; can’t be used after tests
  - Guarantee programmable: if initial fuse resistance <400 $\Omega$
  - Guarantee 100% programmable: if program within specs
  - Fully testable: every functional block, including program circuits

$0.1 \quad $1 \quad $10 \quad $100 \quad $1000

6th FD-SOI Form, Sept. 18, 2018
Beyond 10/7nm: Anti-Fuse(AF)

- MOS can’t sustain high voltage => VDD: 1.2V=>1.0=>0.8=>0.75V
- Oxide can’t be scaled => program voltage can’t be reduced
- Drastically lower channel/junction breakdown after 14nm
- Beyond 10/7nm: MOS breakdown before oxide !!!
- ANTI-FUSE HARD TO WORK !!
- FD-SOI has much lower junction breakdown than bulk

BVJ/BVO: Junction/Oxide Breakdown voltage
Beyond 10/7nm: I-Fuse™

- Beyond 10/7nm: Current PGM prevails voltage PGM !!
- Smaller feature width => lower programming current
- Lower programming current => low programming voltage
- I-fuse™ @22nm FD-SOI: PGM voltage 0.9V, current 1.4mA
- “Non-breaking” I-fuse™ prevails “breaking” eFuse beyond 10/7nm!
OTP: I-Fuse™, eFuse and Anti-Fuse (AF)

- OTP (One-Time Programmable) IP: every chip needs it for tapeout

  - Can be programmed with 1.0V, <1.4mA, for 1-10us
  - Pass 250°C HTS for 1,000hr with cell current variation <5%
  - Read 0.4V/1μA for IoT apps (The only OTP vendor in the world)

- Efuse at 28nm (UMC IEEE IITC/MAM 2011, Intel VLSI 2009 paper)
  - Program Cu in metal-2
  - Need >30mA to program. Can’t pass @150°C HST for 168hr
  - Intel: (IEEE JSSC 4/2010)
    - “read current is only 1/250 of program current”. 100μA =>25mA

- Anti-Fuse (oxide breakdown)
  - @40nm need 5V (G), 6.25V (LP) to program (Kilopass, MPR 6/2010)
  - @32nm HKMG need 4.5V/200us to program (Intel, VLSI Cir Sym., 2012)
  - @14nm FinFET need 4.0V to program (GF, VLSI Tech Sym., 2014)
Conclusions

• Revolutionary I-fuse™ concept: logic device, not NVM
  – Program mechanism can be explained well by physics, NOT chaotic
  – I-fuse™ program behavior can be modeled in HSPICE or Verilog-A
  – I-fuse™ can be synthesized in standard cell library like flip-flops
  – Program 0.9~1.35V & 1mA, not much different from logic device
  – Read 0.4V & 1uA, even below SRAM’s Vddmin
  – No HV circuits. No charge pumps. No exotic charge trapping
  – Cell/IP scalable with Moore’s law, just like any logic device or SRAM
  – Fully testable: can generate complicated test patterns like SRAM
  – Pass 250oC 1Khr qual, just as reliable as any logic devices
  – High data security: accelerate normal device wear-out of logic device

• I-fuse™: the natural OTP of choice
  – I-fuse™ is a logic device. Doesn’t need to be qualified like an NVM
  – When a logic process is qual’d by SRAM, I-fuse™ is qual’d
  – Save tremendous amount of time, costs, and efforts to industry !!!
BACKUP
**Electro-migration**

**Rupture**

**Melt**

**Defect: 1E-5 (IBM)**

**Gate oxide Breakdown**

**Hard breakdown**

**Soft breakdown**

**Ultra-Thin Gate Dielectrics: They Break Down, But Do They Fail? IEDM 97-73**

We study breakdown in high-quality 2-7nm gate dielectrics, and find that soft breakdown becomes more likely for thinner oxides and for oxides stressed at lower voltages. For 2nm oxides, an increase in gate noise is the only precise indication of soft breakdown. For many applications, devices should remain functional with the level of gate noise we have observed, after soft breakdown.

**Logic EPROM**

- Only good for 0.35/0.5um CMOS
- Data retention
IoT Is Data Security

- Which I-fuse™ at GF 28nm has been programmed?
  - Heck a fuse 90%, hack 1Kb ~ 0 (0.91,000 = 1.39E-47) !!
About Attopsemi

- Founded in June 2010
  - By a team of semiconductor veterans and experts
- Located at Si-Soft Research Center of Hsinchu Science Park, Taiwan
- Biz: OTP (One-Time Programmable) IP development & licensing
  - Foundry independent OTP; no additional masks or process steps
  - Program not by NVM ways: blow fuse, rupture oxide or trap charges
  - But by “true electromigration: accelerating wear-out of logic devices”
    - 100x reliability, 1/100 cell size, and 1/10 program current of eFuse
    - Pass HTS at 300°C for 4,290hr; defect rate <0.01ppm
  - Universal and proven OTP from 0.7um to 22nm and 7nm and beyond
- Patent portfolio: >65 filed in US and 11 in Taiwan/China
- Engaged >5 foundries and >50 customers worldwide
The Team

• **Founder**: Shine Chung
  • Harvard graduate in Applied Physics
  • 30 years of IC design experience
  • Memory design in AMD, Intel, and HP
  • PA-WW architect (PA-WW: precedent of Intel’s Merced)
  • Director at TSMC (eFuse pioneer)
  • VLSI and ISSCC technical committee member for 4 years
  • Two-time TSMC innovation award recipient
  • More than 61 US patents granted before Attopsemi
  • Filed more than 65 U.S. patents at Attopsemi Technology

• **Co-founder & VP of Eng**: WK Fang
  • MSEE from Ann Harbor, U. of Michigan
  • 20 years of experiences in memory
  • Technical Manager at TSMC
  • Department Manager for eFuse
  • Design manager for N90/N65 SRAM TV, eDRAM
  • MTS in SRAM, FIFO, CAM at IDT
What’s I-fuse™ vs eFuse?

- **Non-breaking fuse**: Program below a critical current $I_{\text{crit}}$ and above electromigration (EM) threshold*
- Deterministic programming
- => **ultra-high reliability**

- **Breaking fuse**: Program beyond a critical current
- Explosive programming
- => debris grow back

**Figure 3.** 1-V characteristics of a typical element upon programming.

Any Power Devices would prevent operating under “thermal run away.” Why a fuse under such condition can be reliable?

* US patents granted
We made OTP history: the only OTP passes HTS 300°C, 4,290hr
96 dies of 4Kx8 (3Mb I-fuse™) at 0.16um HV pass HTS 300°C, 4Khr
   No defect found and no redundancy in use
Cell current variation after stress vs. before stress
   Cell current changes <5% after baking
400°C 8hr I-Fuse™ Bake

- I-fuse™ cell current variation <5% after HTS 400°C for 8hrs
  - Passing 400oC for >2hr is a must in RDL process for 3D IC
  - Foundry eFuse can’t pass 400°C for 2hrs, with 20-30 defects in 1Mb
  - 96 4Kx8 I-fuse™ dies @0.16um HV passed @400°C (0 defects in 3Mb)
Myths about OTP

- OTP market size too small
  - All chips need OTP
  - 1% of royalty for $300B worldwide market means $3B
  - Majority of OTP in use are in-house eFuse
- OTP is an NVM memory and should be qual’d like an NVM
  - Existing OTPs are NVMs: break fuse, rupture oxide, & trapping charges
  - Innovative I-fuse(tm) OTP: non-breaking fuse: a logic device
- Conventional eFuse programming is based on electromigration (EM)
  - A mixed of EM/rutpure/decompose/melt under thermal runaway
- Breaking a fuse is more reliable
  - Breaking a fuse by explosion ISN’T; Raising fuse resistance by EM IS
- High post- and pre-program fuse resistance ratio is a figure of merit
  - 5X or 10X resistance ratio is good enough for sensing
- OTP needs redundancy
  - OTP should have high yield and high reliability. Needs no redundancy